

COMPAL CONFIDENTIAL

MODEL NAME : VAL90

PCB NO : DA6000WZ010

GPIO P/N: 2012.8.1 Rev 2.7

BOM P/N :

X76 of SPI:

X7650731L03

SA000039A30 (64M W25Q64FVSSIQ)

SA00003K820 (32M W25Q32FVSSIQ)

X7650731L04

SA00006N000 (32M MX25L3273EM2I-10G)

SA00006N100 (64M MX25L6473EM2I-10G)

SALADO 14 HSW UMA

HASWELL + LYNX POINT

2013-07-04

REV : 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

SPI@ : For X76 SPI

14UMA

EMC@: EMI/RF/ESD ask to add V

CXDP@ : CPU XDP


PXDP@ : PCH XDP

COMPRESSED IMAGE

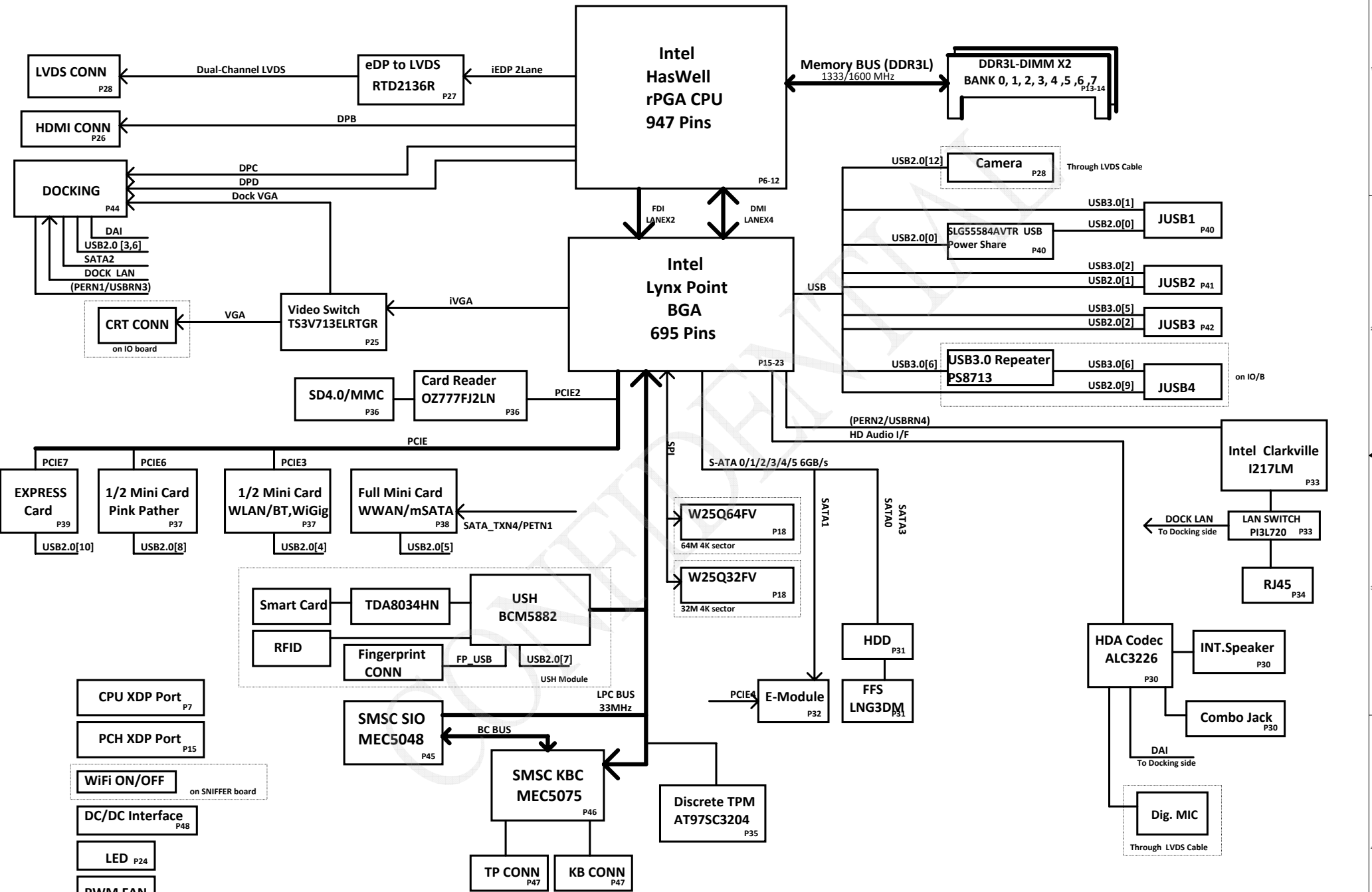
MB PCB	
Part Number	Description
DA6000WZ000	PCB 0YG LA-9931P REV0 M/B UMA 6

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Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB 2.0 PORT#	USB 3.0 PORT#	DESTINATION
	0	1	Rear Side (JUSB1)
	1	2	Right Side TOP (JUSB2)
	2	5	Right Side bottom (JUSB3)
	3	3 (PERN1/USBRN3)	DOCKING (JDOCK1)
	4		WLAN (JMINI2)
	5		WWAN (JMINI1)
	6		DOCKING (JDOCK1)
	7		USH (JUSH1)
	8		Pink Pather (JMINI3)
	9	6	Left Side (JUSB4)
	10		Express card (JEXP1)
	11		None
	12		CAMERA (JCAM1)
	13		LCD Touch

PCI EXPRESS	DESTINATION
Lane 1 (SATA_TXN4/PETN1)	WWAN (JMINI1) SATA by default
Lane 2 (SATA_RXN5/PERN2)	None
Lane 2 (PERN2/USBRN4)	10/100/1G LOM
Lane 3	WLAN (JMINI2)
Lane 4	E3 Module Bay (JSATA2)
Lane 5	None
Lane 6	Pink Pather (JMINI3)
Lane 7	Express card (JEXP1)
Lane 8	MMI

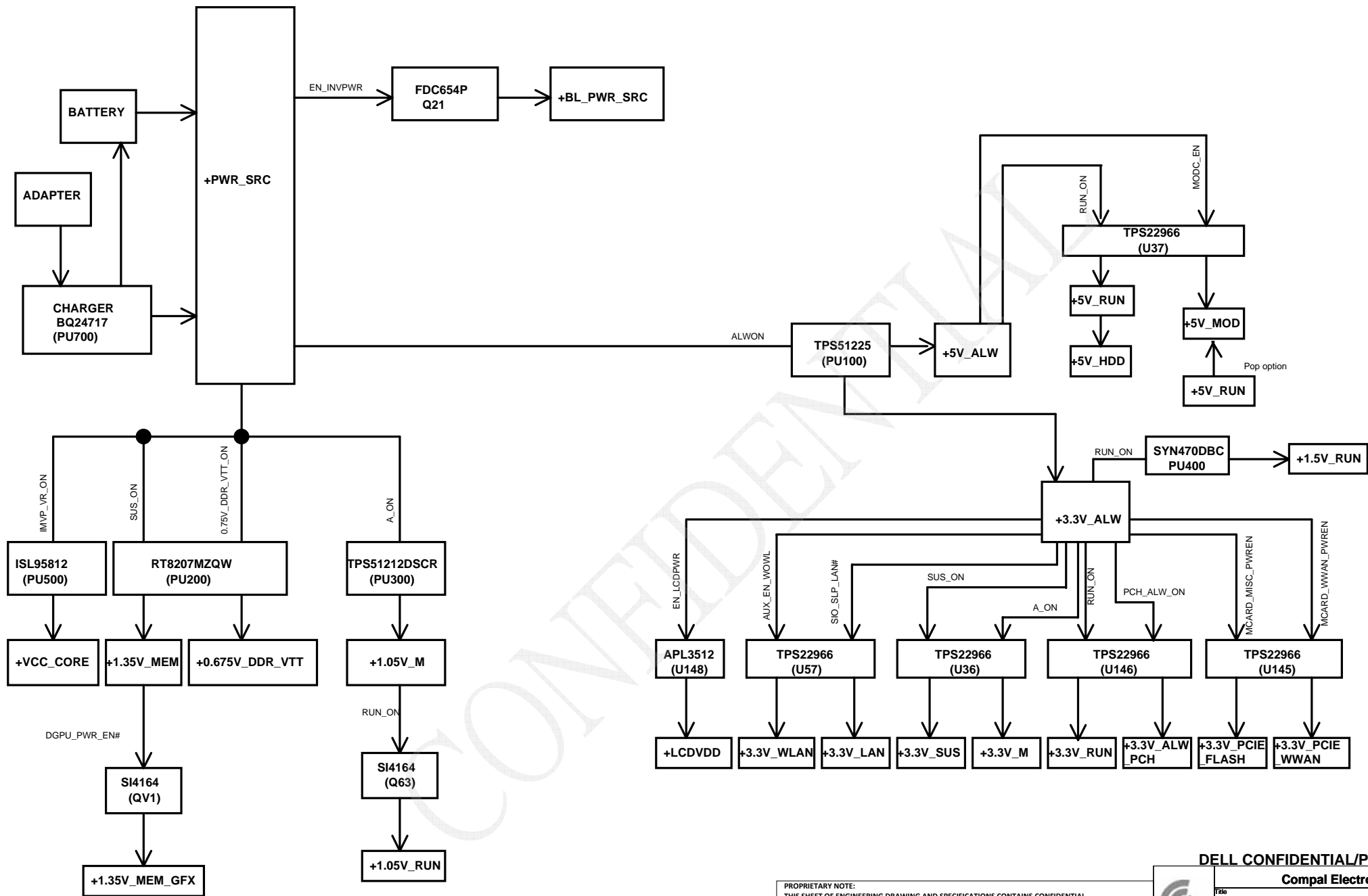
SATA	DESTINATION
SATA 0	HDD (JSATA1)
SATA 1	ODD (JSATA2)
SATA 2	Dock (JDOCK1)
SATA 3	NA
SATA 4 (SATA_TXN4/PETN1)	WWAN (JMINI1) SATA by default

DISPLAY Ports On CPU	Connetion
DDIB	MB HDMI (JHDMI1)
DDIC	Dock DP port 1
DDID	Dock DP port 2

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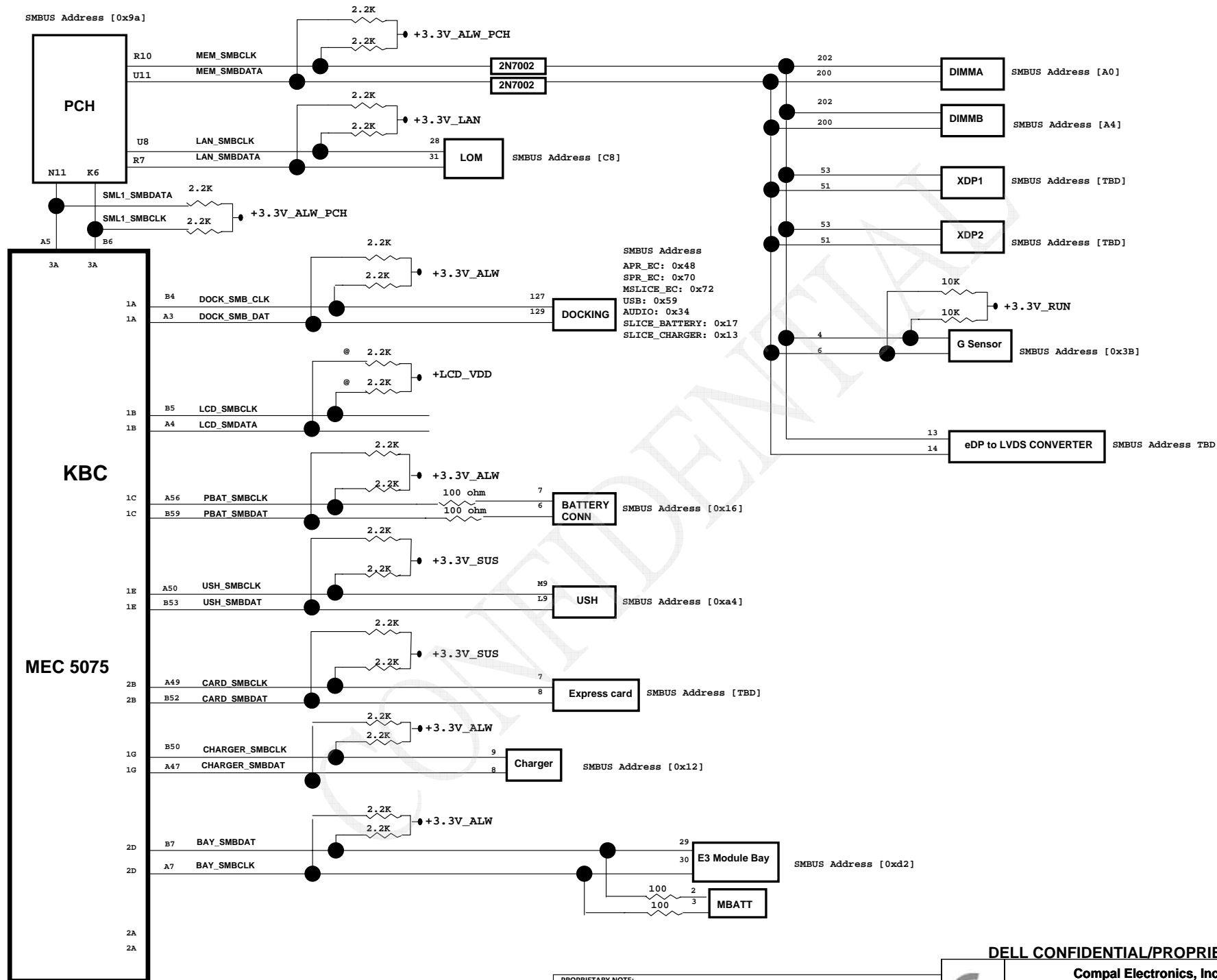
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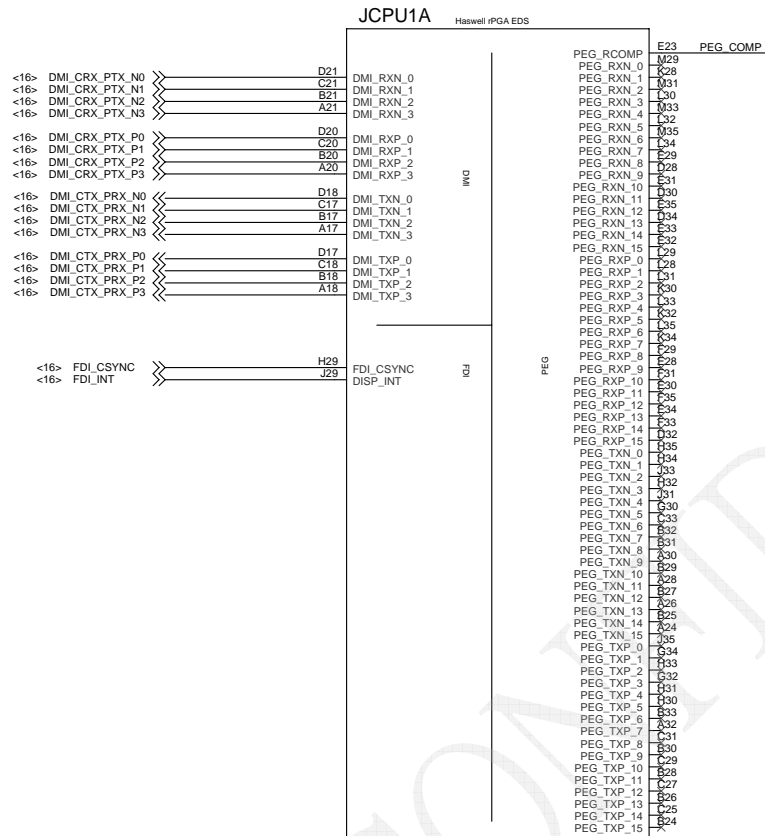
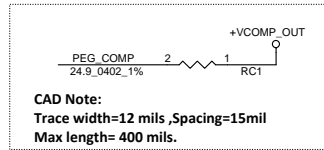
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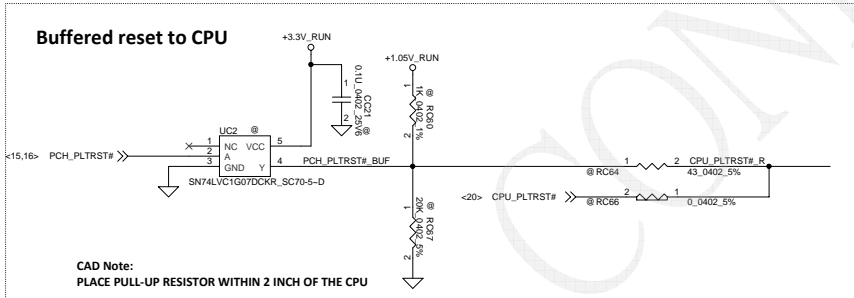
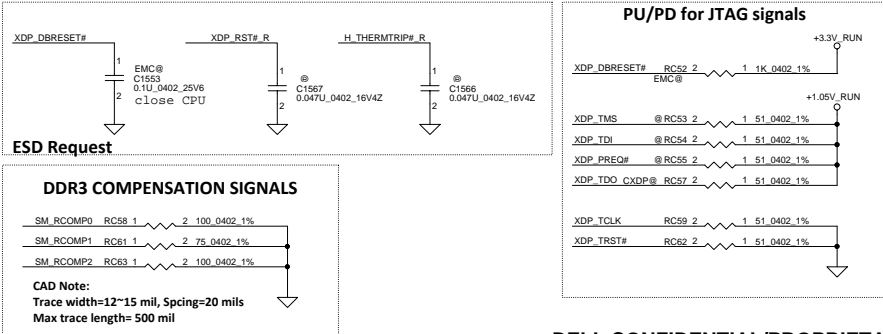
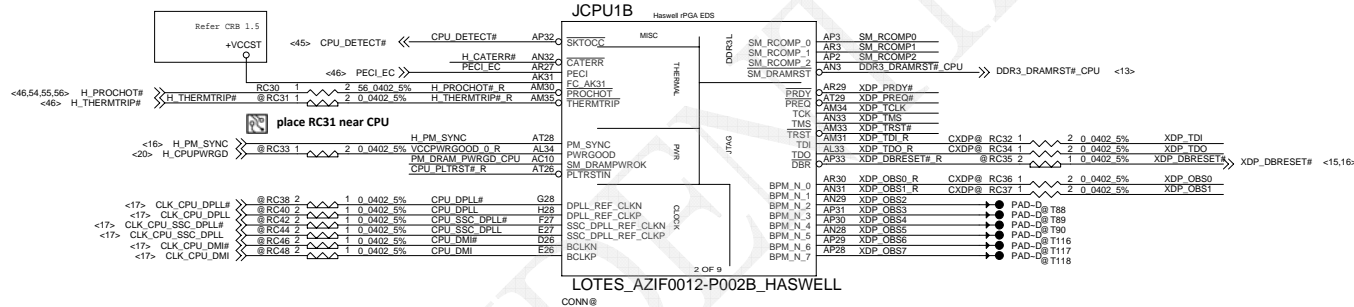
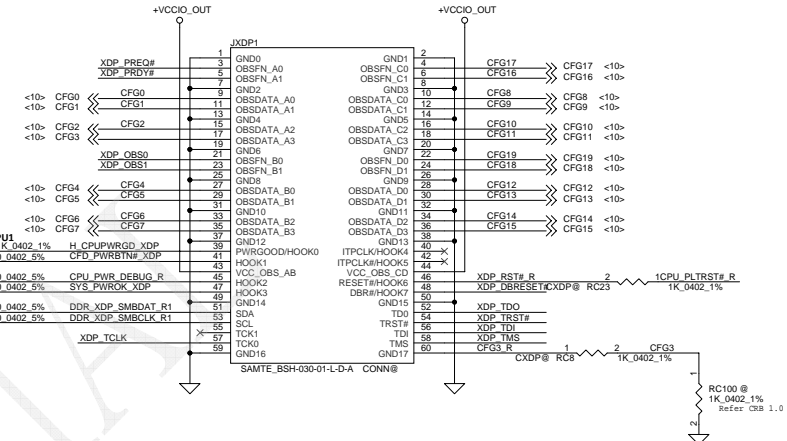
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[illegible]

CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC33 & RC56

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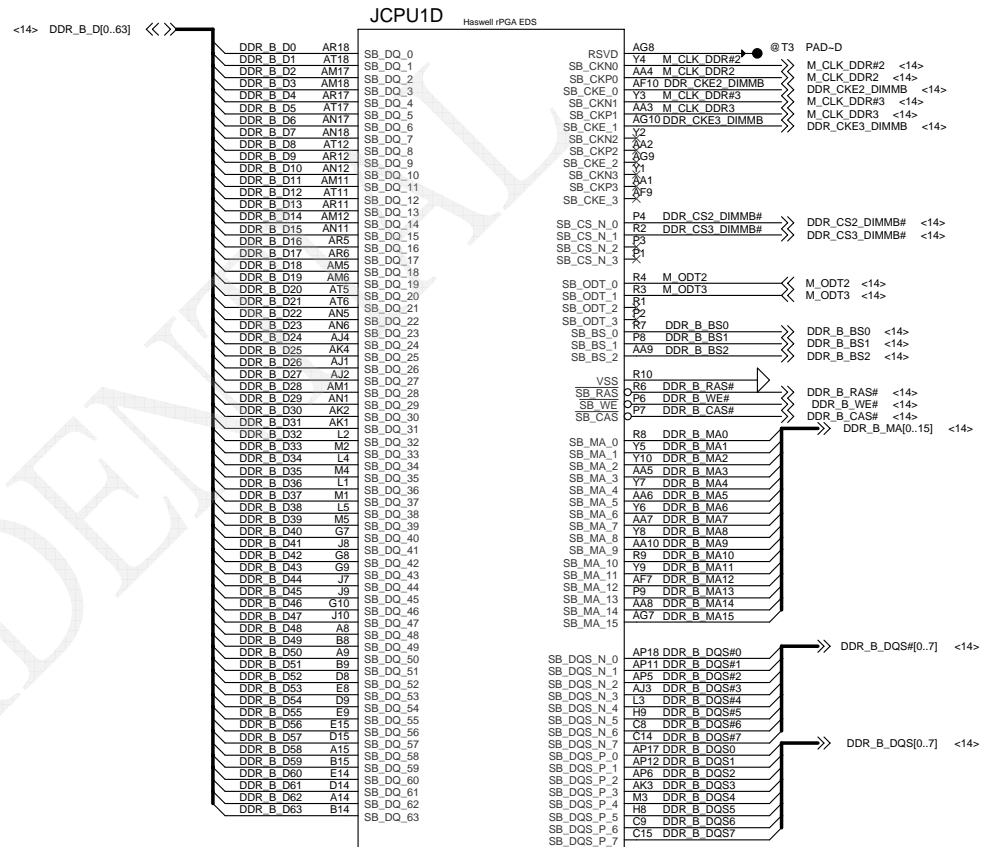
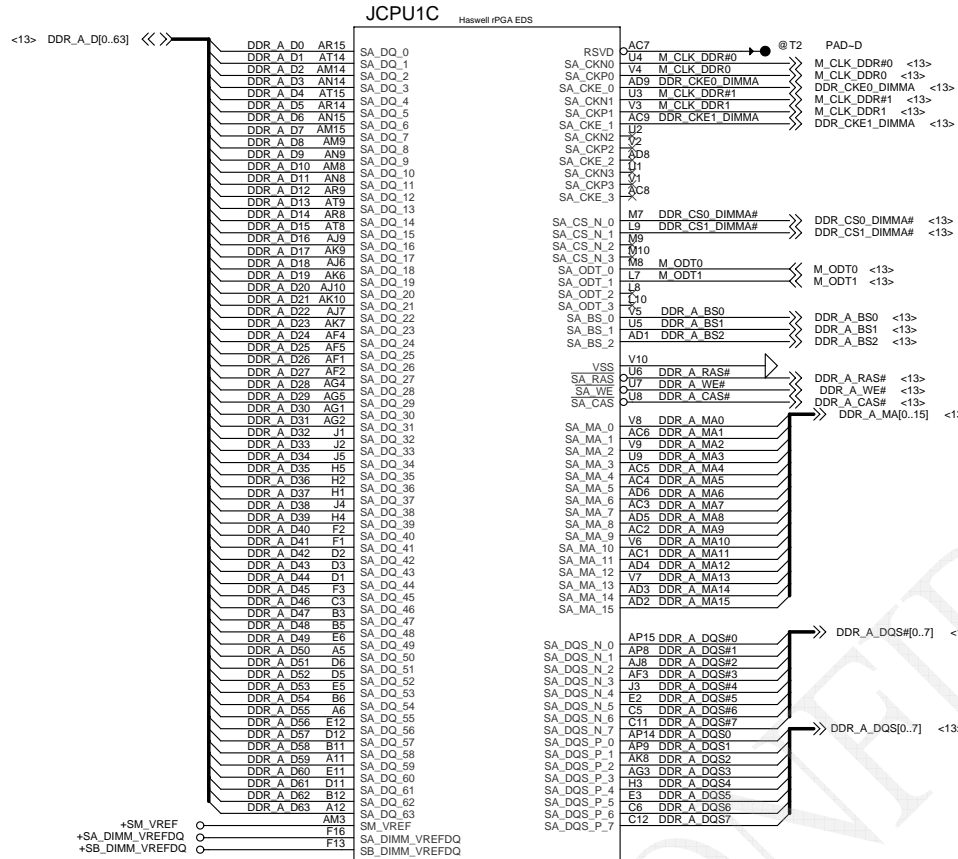
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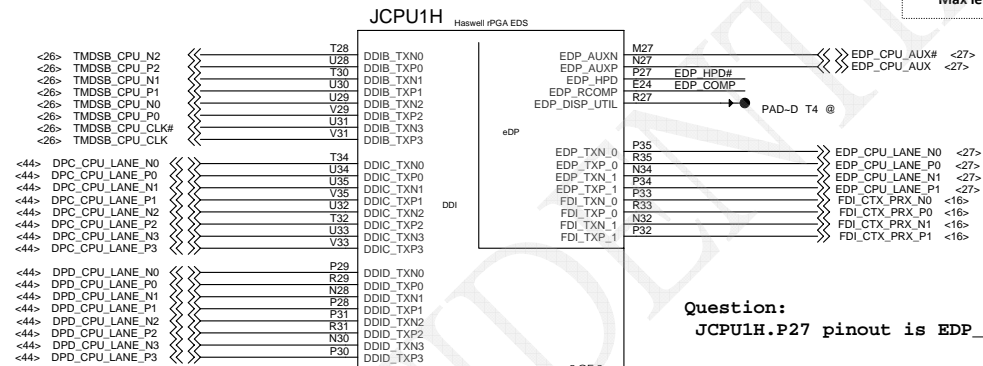
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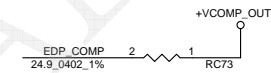
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CONN@

COMPENSATION PU FOR eDP

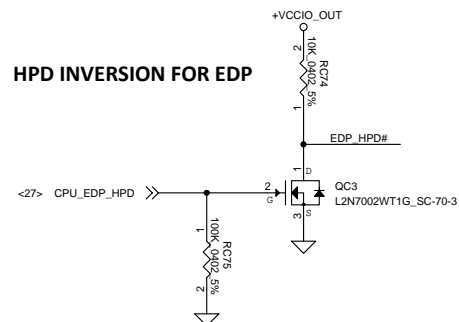


CAD Note: Trace width=20 mils, Spacing=25mil, Max length=100 mils.

Question:

JCPU1H.P27 pinout is EDP_HPD. is it high active when Plug in eDP device?

HPD INVERSION FOR EDP



QC3 change PN to SB50138003L S TR BSS138-7-F 1N SOT23-3

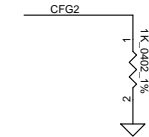
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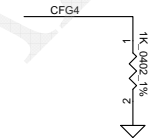
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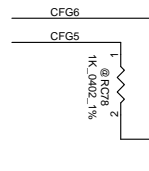
CFG STRAPS for CPU



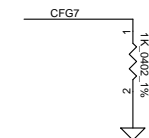
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



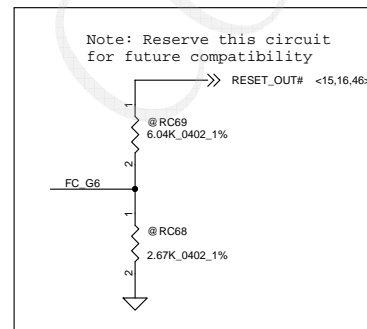
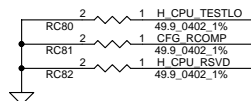
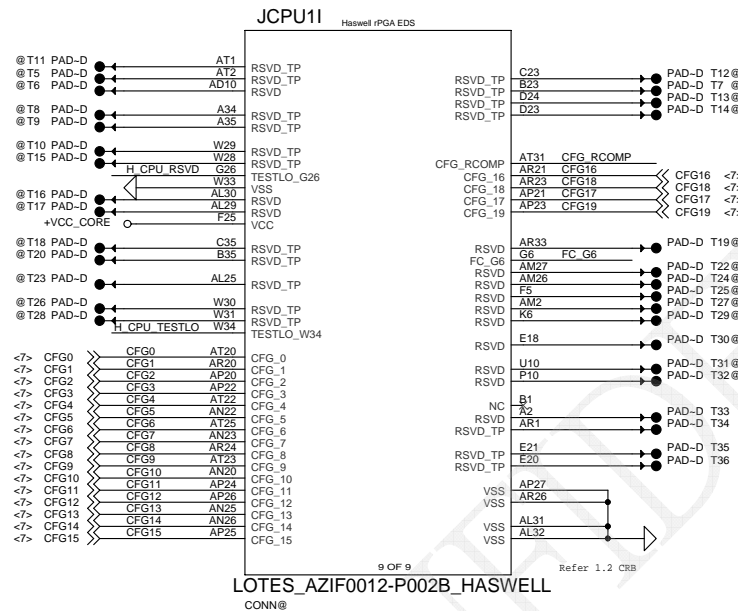
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



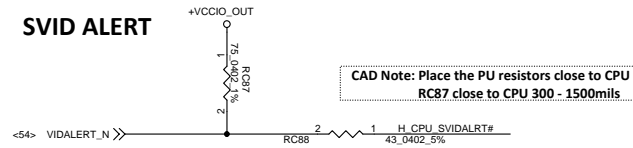
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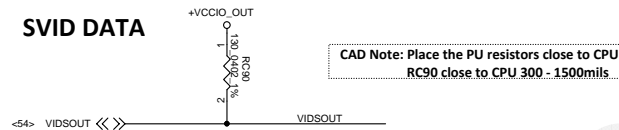
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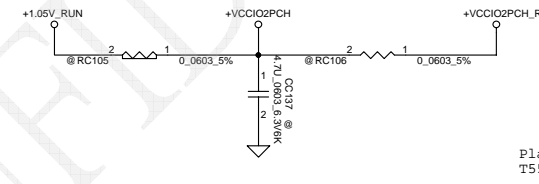
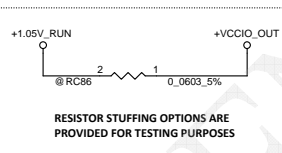
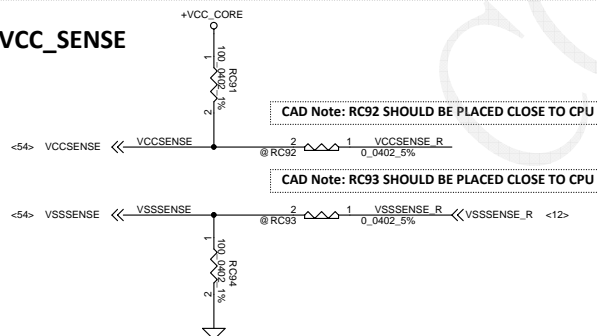
SVID ALERT



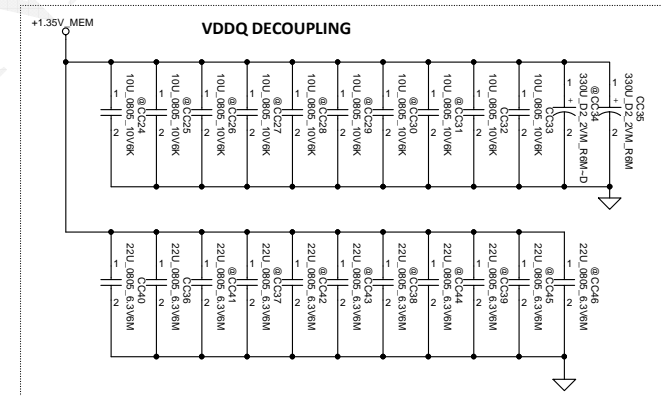
SVID DATA



VCC_SENSE

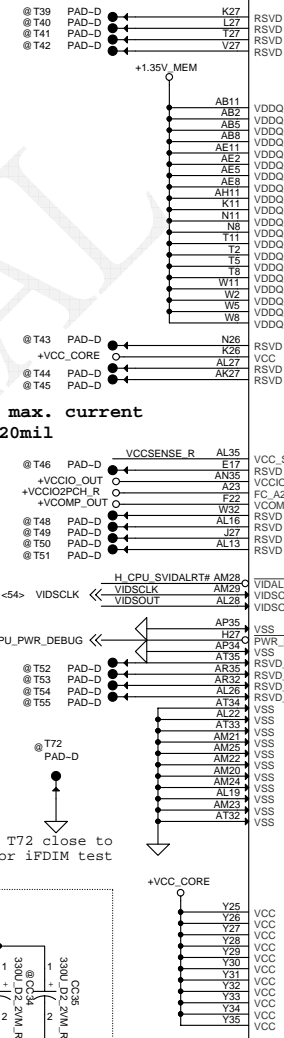


VDDQ DECOUPLING



JCPU1E

Haswell rPGA EDS



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CONN@

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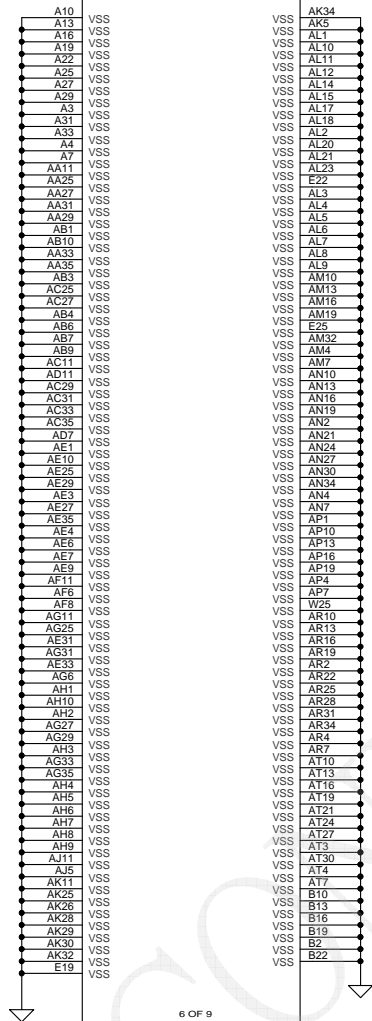
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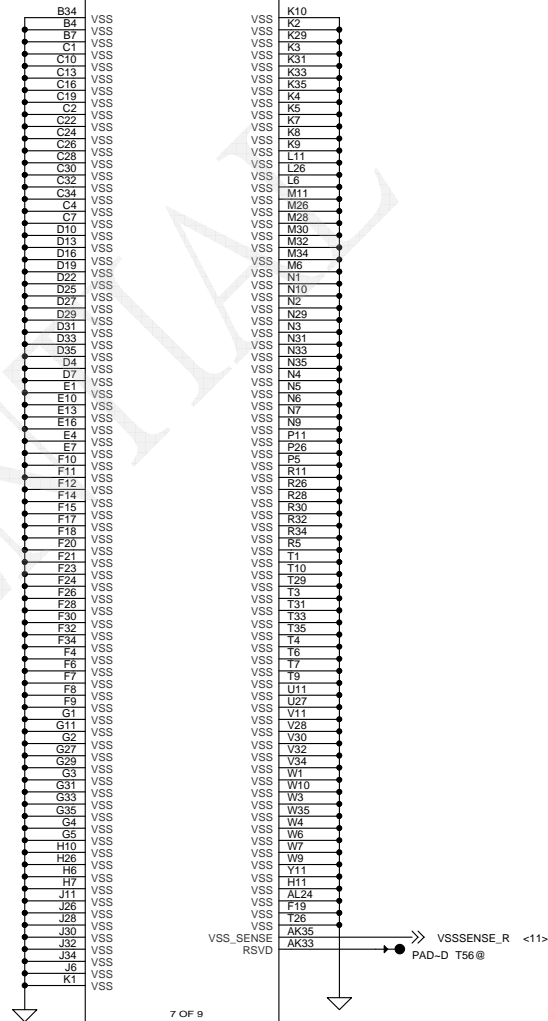
JCPU1F

Haswell rPGA EDS

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JCPU1G

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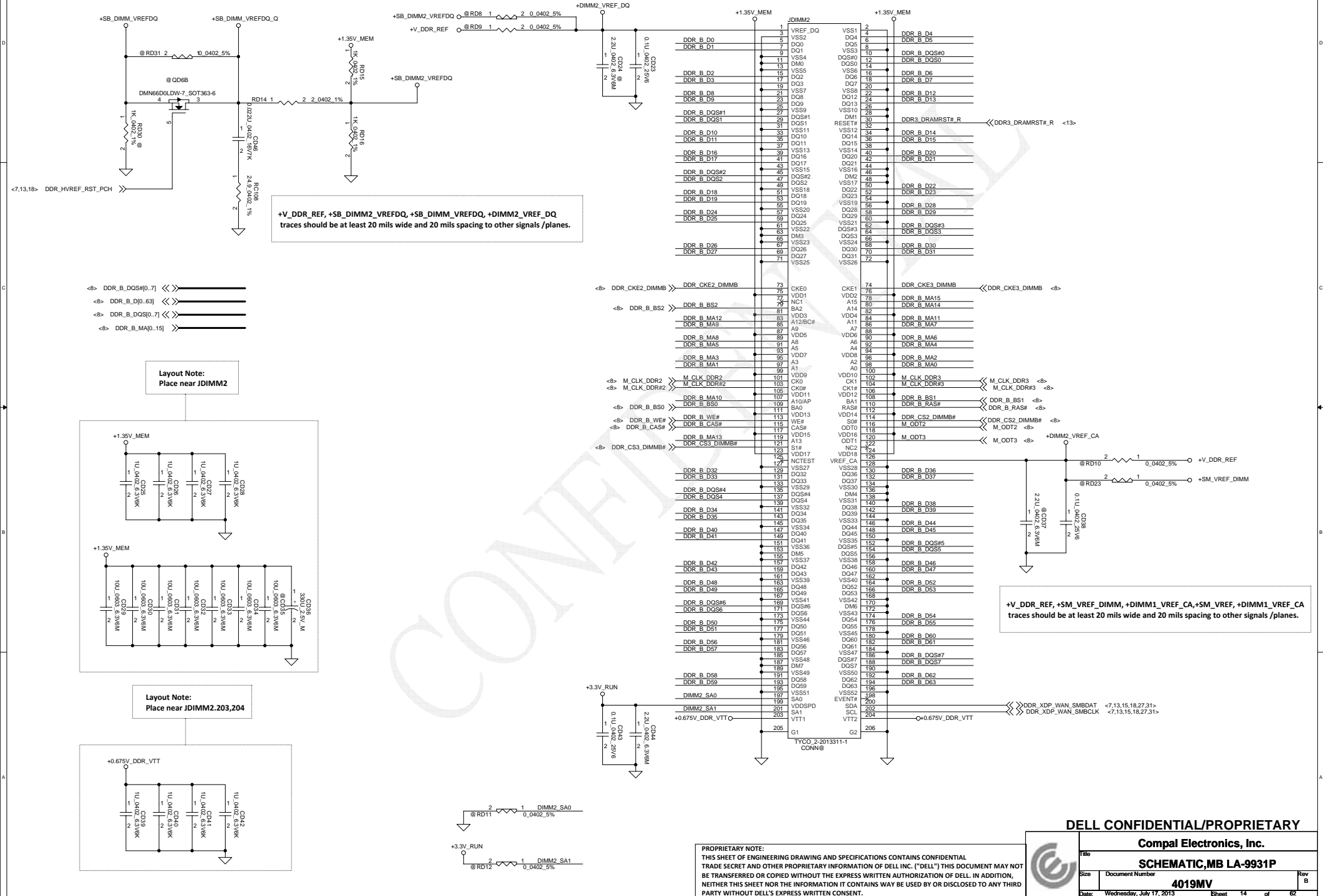
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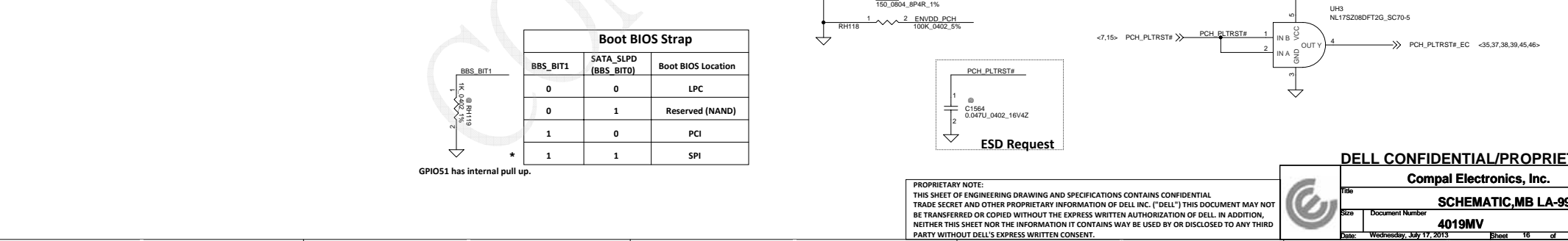
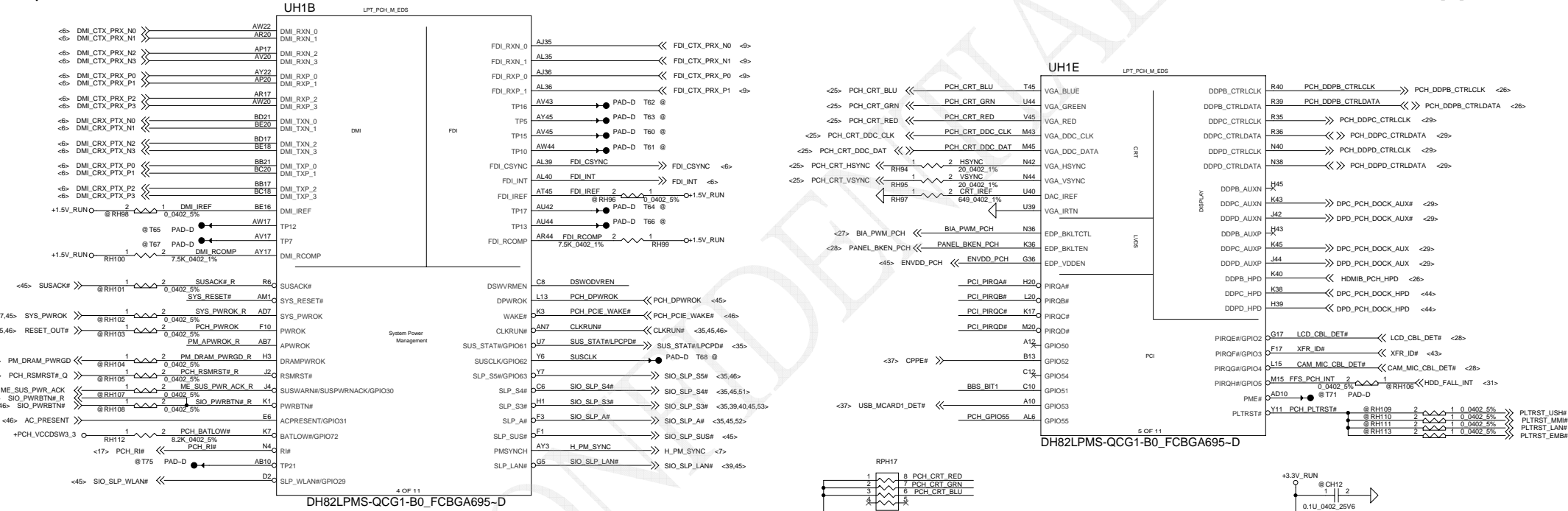
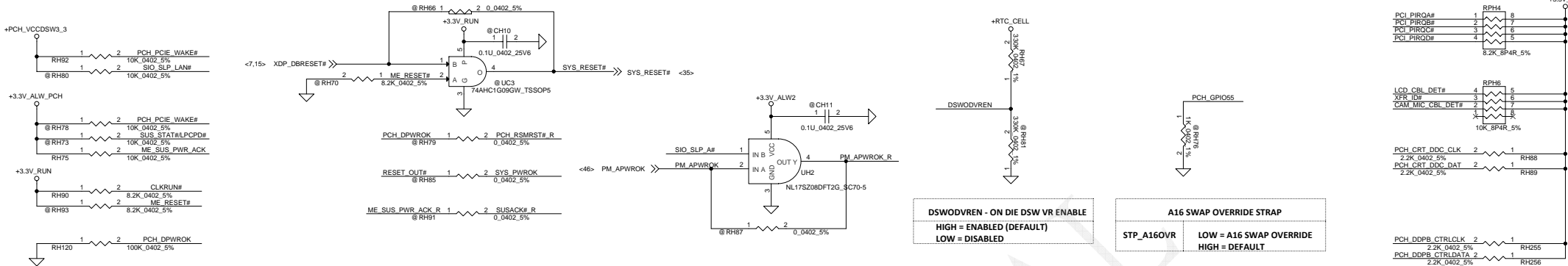
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Populate RD4, De-Populate RD9 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M3

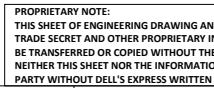
JDIMM2 H=9.2mm





Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

GPIO51 has internal pull up.



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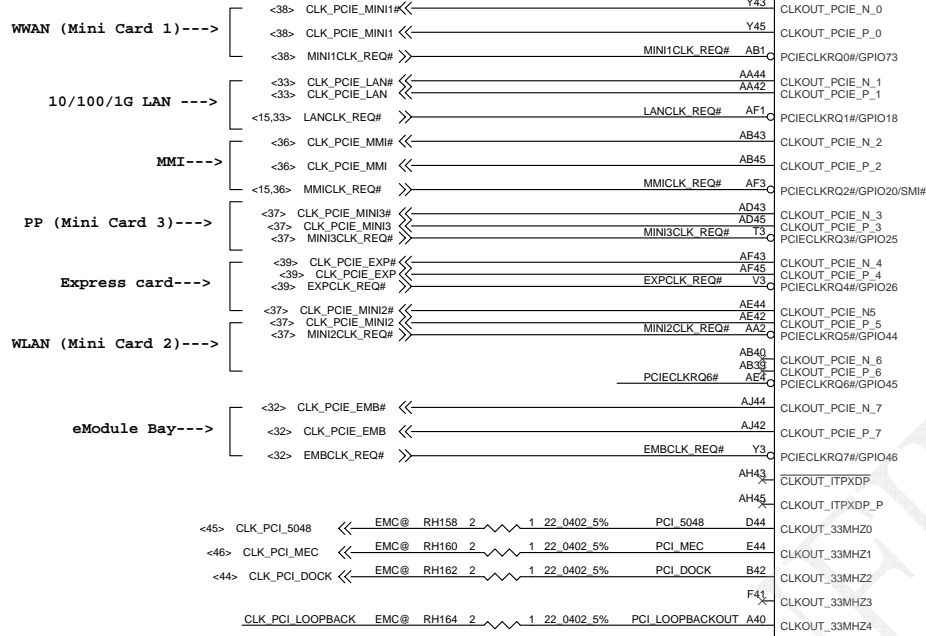
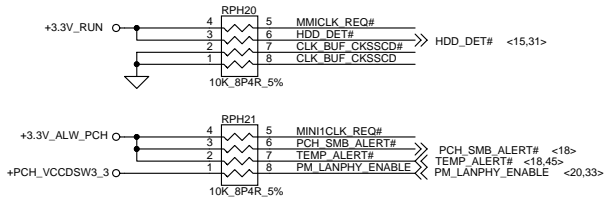
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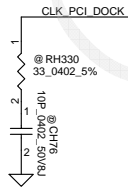
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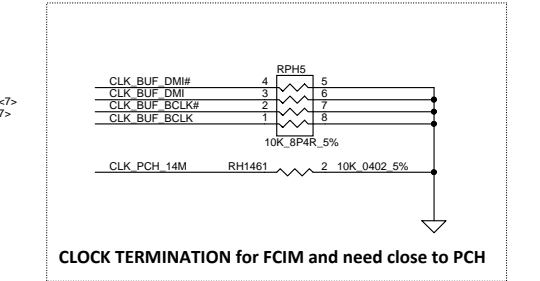
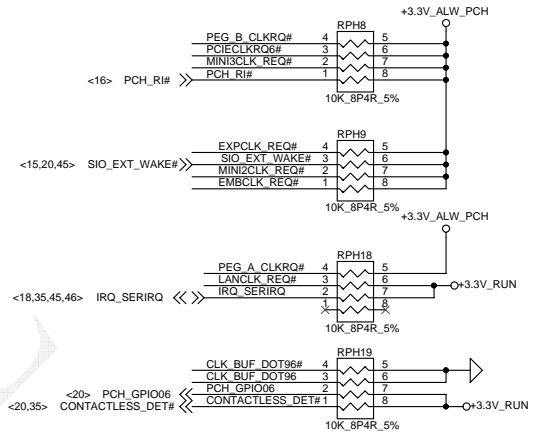
PCIECLK REQ Pull UP Power Rail:
SUS Rail : 0 3 4 5 6 7
Core Rail: 1 2



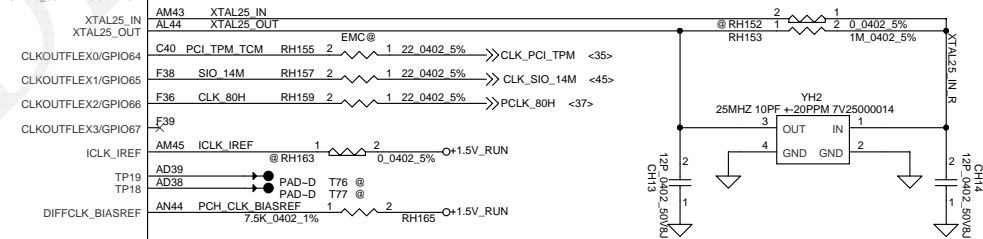
UH1C

LPT_PCH_M_EDS

2 OF 11
 DH82LPMS-QCG1-B0_FCBGA695-D



CLOCK TERMINATION for FCIM and need close to PCH



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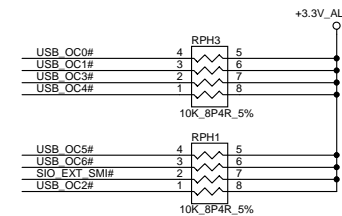
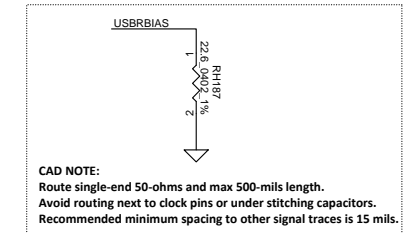
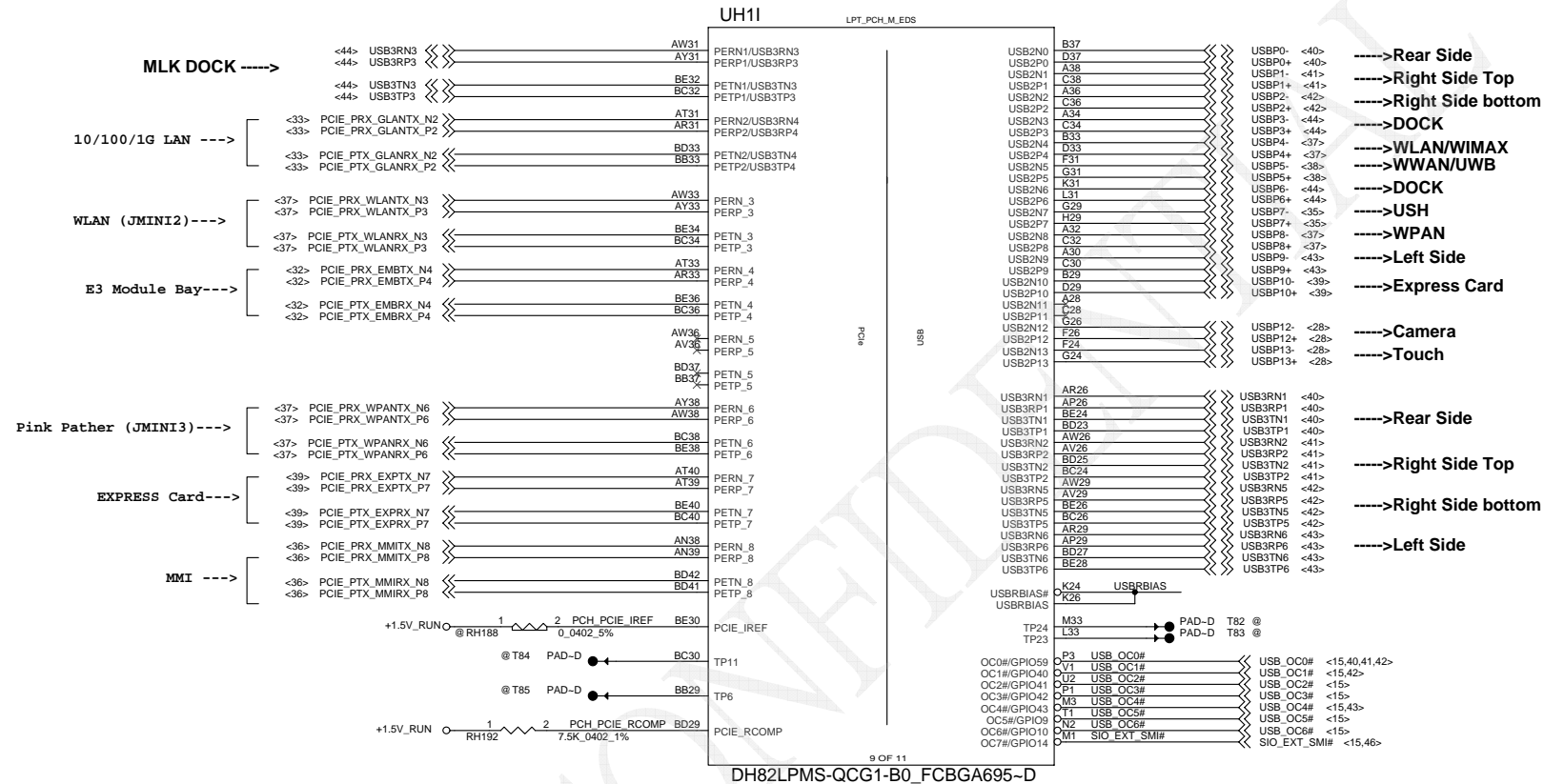
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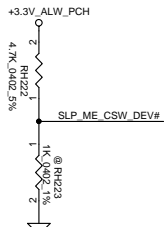
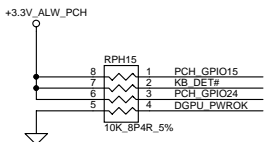
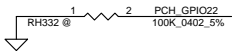
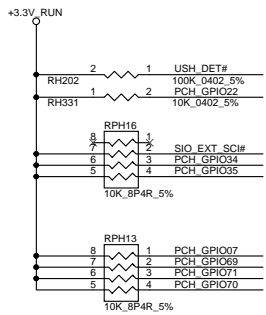
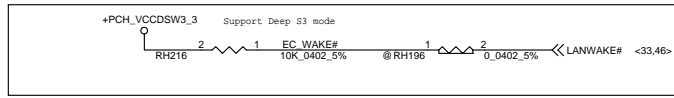


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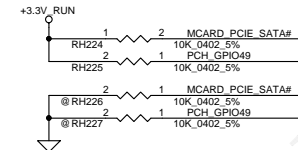
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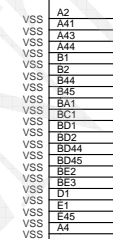
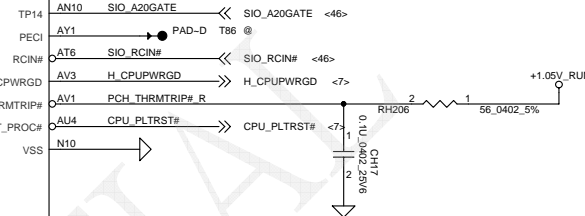
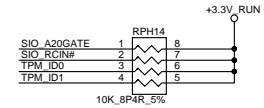
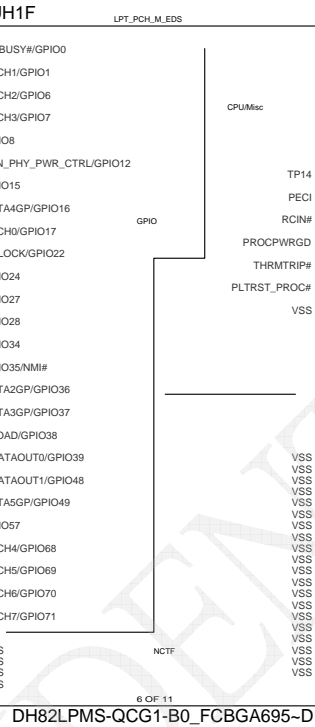
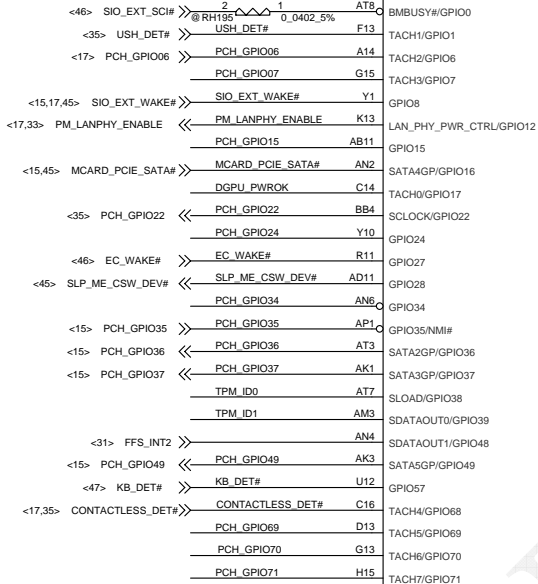
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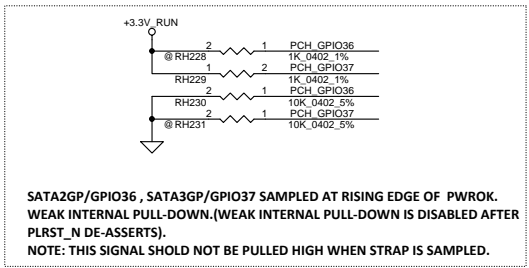
PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW



Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01



CRB1.2 already change to GND directly at UH1.A44, B45, BD1 pins




SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

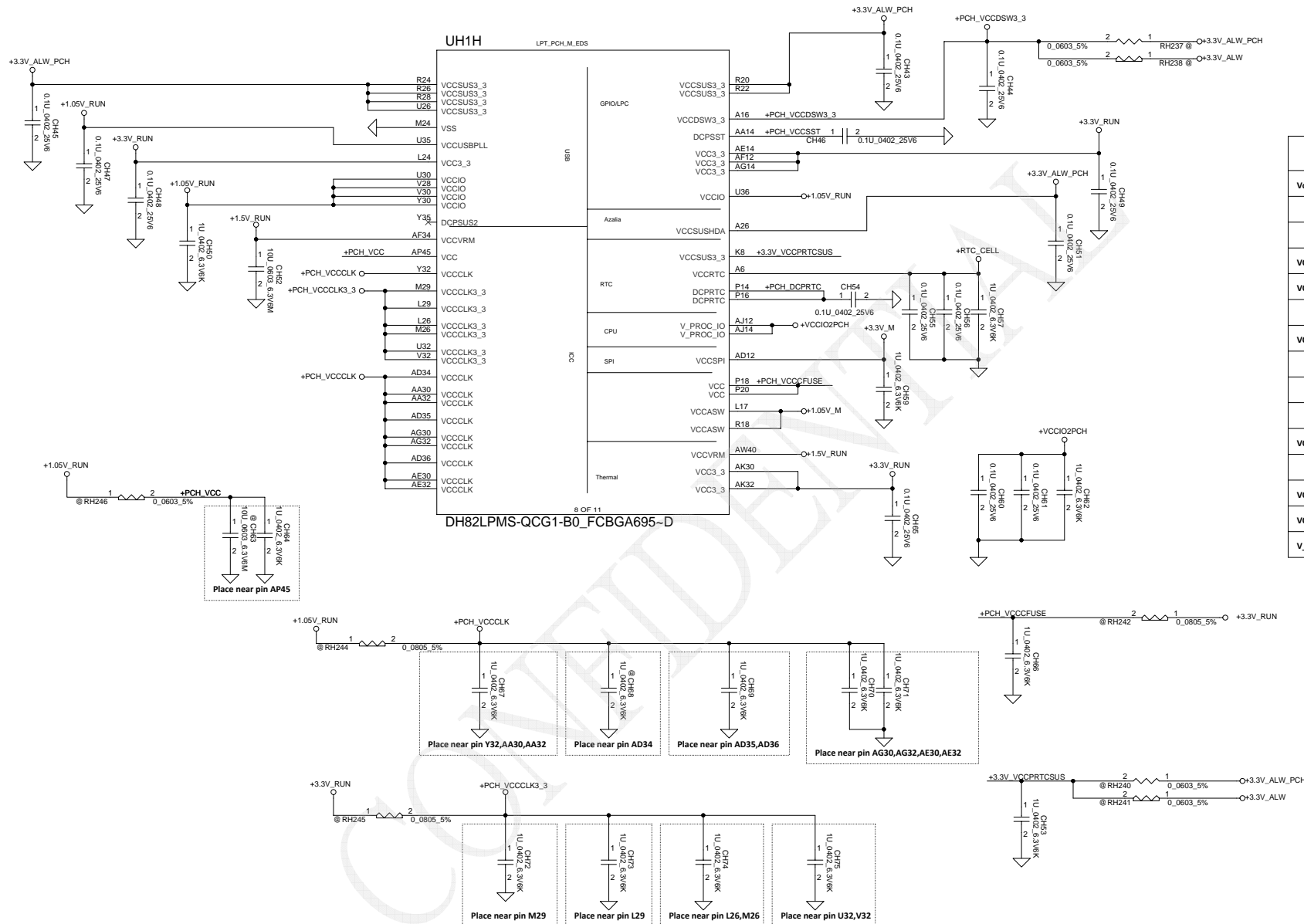
Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals					
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)							(00)	(00)						
				USB3 3	USB3 4							PCIE 1	PCIE 2						
				(01)	(01)							(01)	(01)						

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PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.138 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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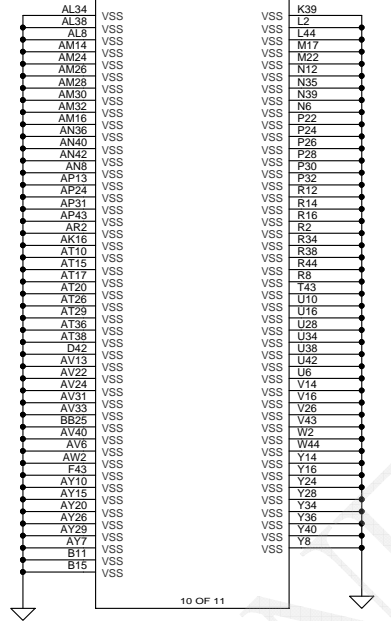
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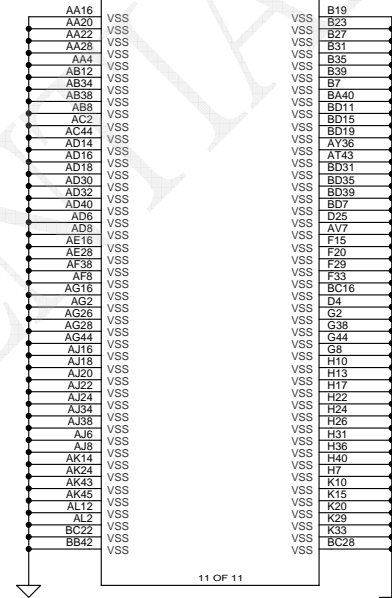
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UH1J LPT_PCH.M.EDS



DH82LPMS-QCG1-B0_FCBGA695~D

UH1K LPT_PCH.M.EDS



DH82LPMS-QCG1-B0_FCBGA695~D

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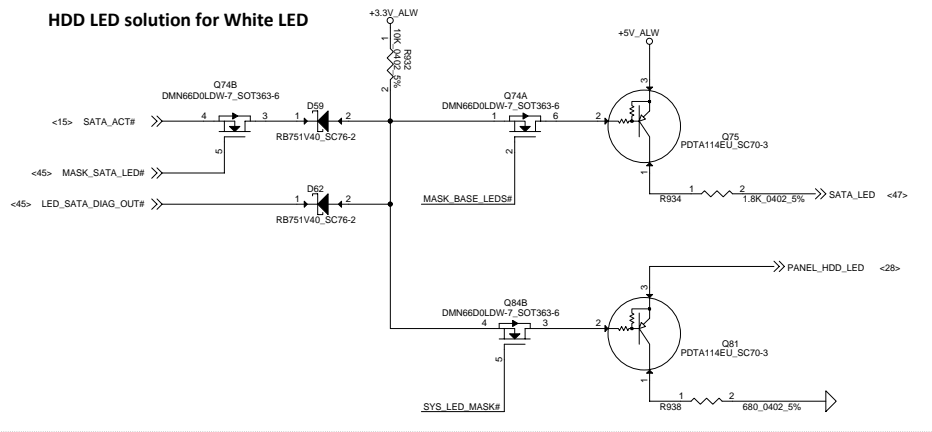


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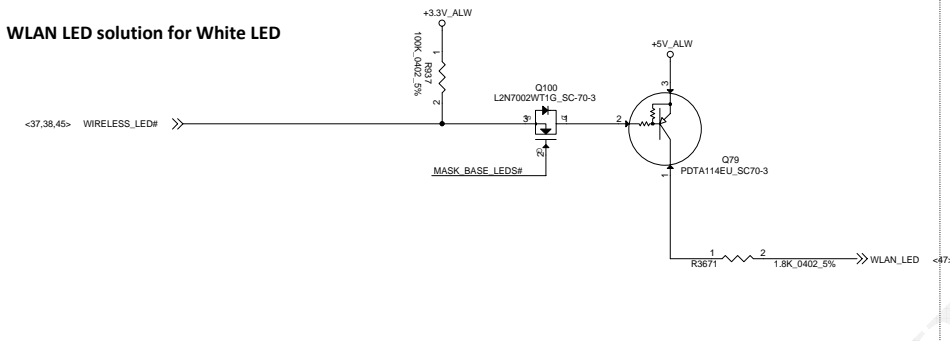
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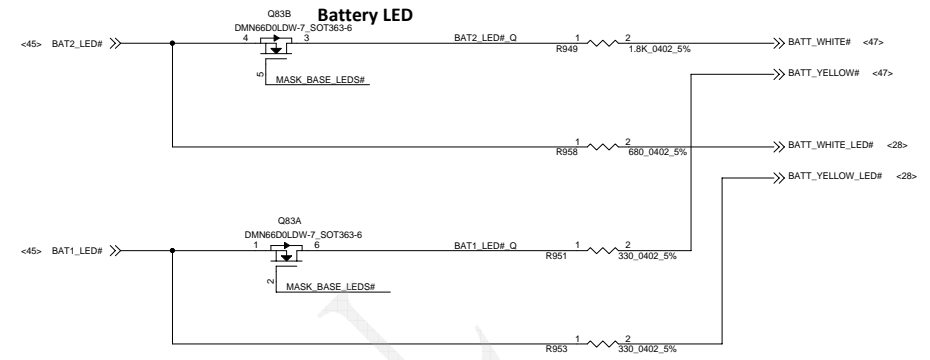
HDD LED solution for White LED



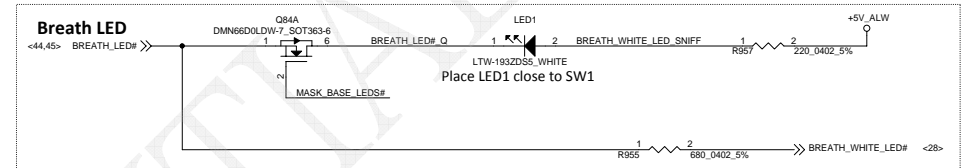
WLAN LED solution for White LED



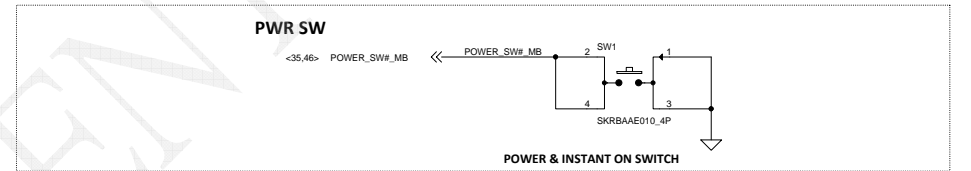
Battery LED



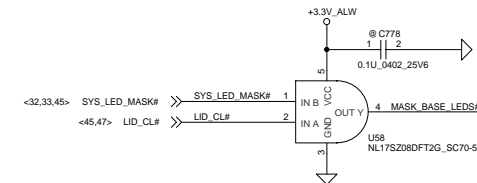
Breath LED



PWR SW

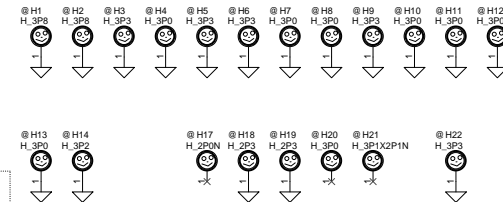


POWER & INSTANT ON SWITCH



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



Fiducial Mark



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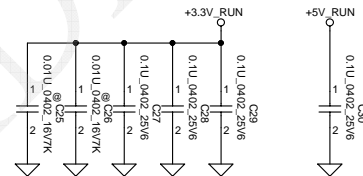
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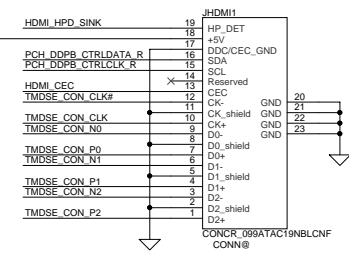
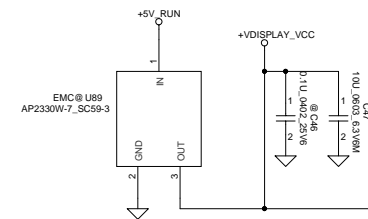
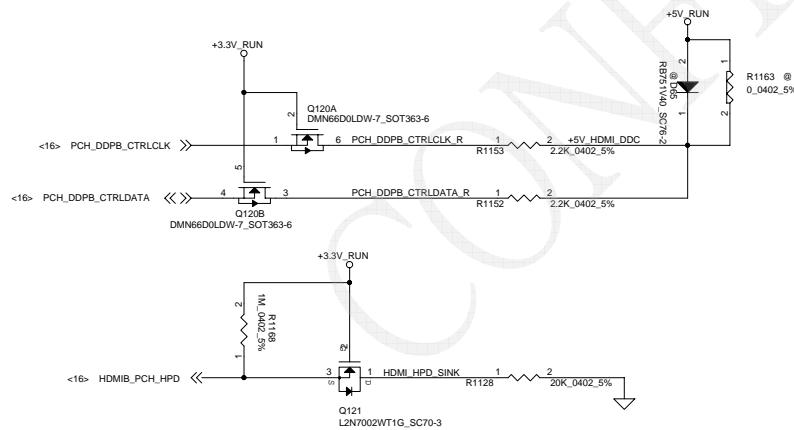
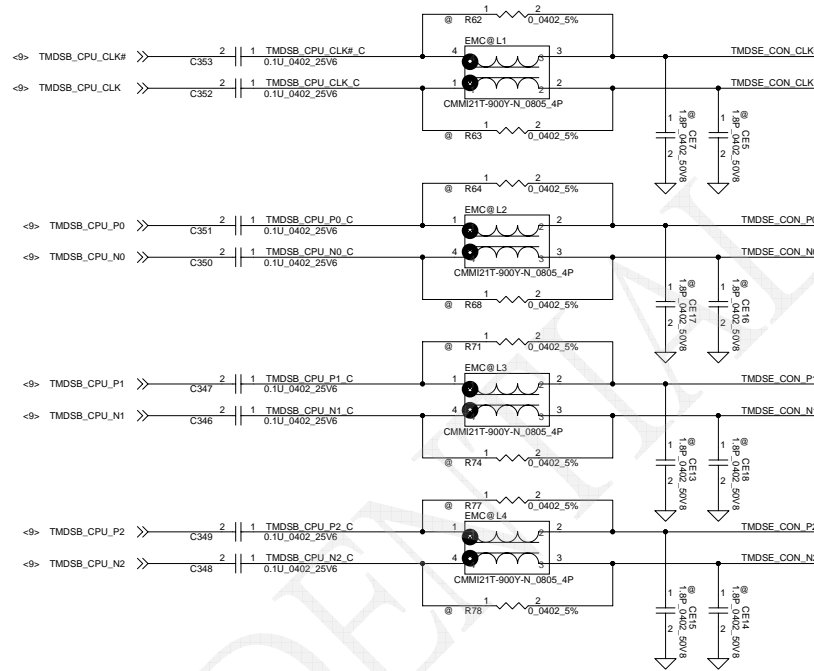
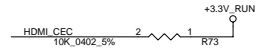
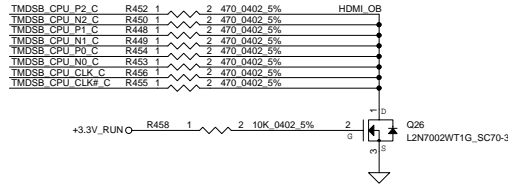
Pin connection diagram for the TS3V713ELTGRN_TQFN32_6x3 package. The diagram shows the mapping of external signals to the package pins. On the left, external signals include <16> PCH_CRT_RED, <16> PCH_CRT_GRN, <16> PCH_CRT_BLU, <16> PCH_CRT_HSYNCR, <16> PCH_CRT_VSYNCR, <16> PCH_CRT_DDC_DAT, <16> PCH_CRT_DDC_CLK, <45> CRT_SWITCH, +3.3V_RUN0, and +3.3V_RUN. On the right, external signals include RED_CRT <43>, GREEN_CRT <43>, BLUE_CRT <43>, VSYNCR_BUF <43>, VSYNCR_BUF <43>, DAT_DDC2_CRT <43>, CLK_DDC2_CRT <43>, RED_DOCK <44>, GREEN_DOCK <44>, BLUE_DOCK <44>, VSYNCR_DOCK <44>, VSYNCR_DOCK <44>, DAT_DDC2_DOCK <44>, and CLK_DDC2_DOCK <44>. The package pins are numbered 1 through 33. Pin 1 is R, 2 is S, 3 is VDD, 4 is VDD, 5 is VDD, 6 is H_SOURCE, 7 is V_HOUCR, 8 is SDA_SOURCE, 9 is SCL_SOURCE, 10 is SEL, 11 is TEST, 12 is Reserved, 13 is GND, 14 is GND, 15 is GND, 16 is GND, 17 is GND, 18 is GND, 19 is GND, 20 is GND, 21 is GND, 22 is GND, 23 is GND, 24 is GND, 25 is GND, 26 is GND, 27 is GND, 28 is GND, 29 is GND, 30 is GND, 31 is GND, 32 is GND, 33 is GND. The package is labeled TS3V713ELTGRN_TQFN32_6x3.

SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



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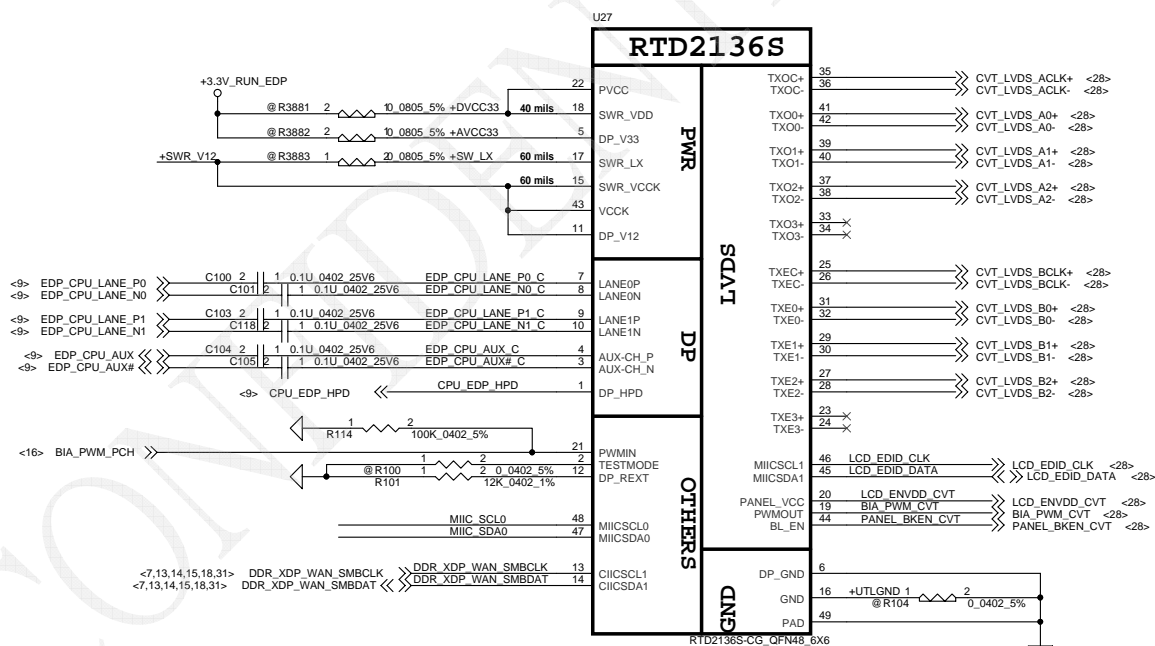
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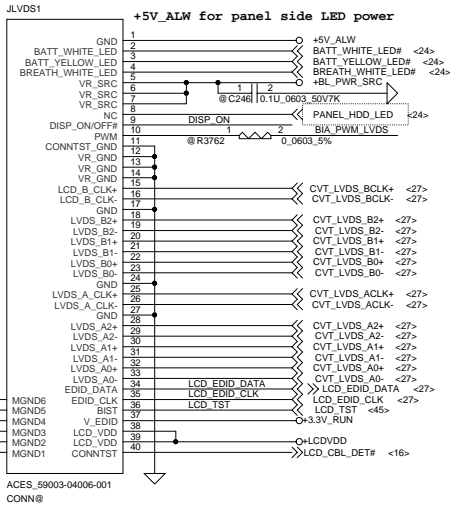


Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA

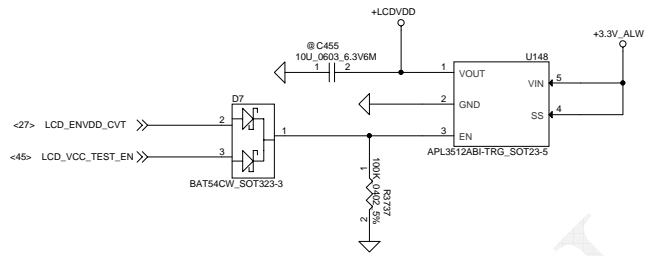
*** 2. RTD2136R SA000067100 : De-Populated R102, R103, R107; Populate R108;

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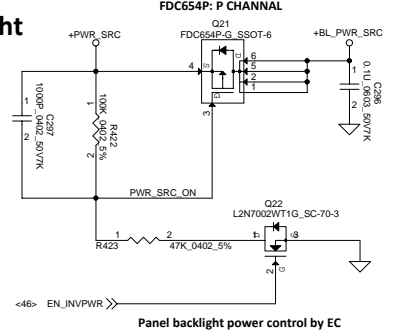
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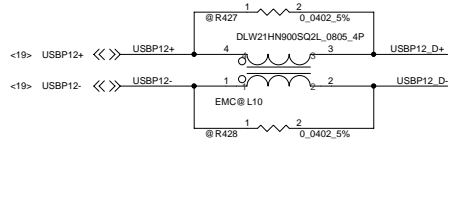
LCD Power



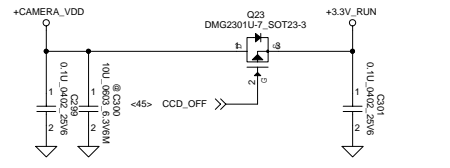
LCD Backlight



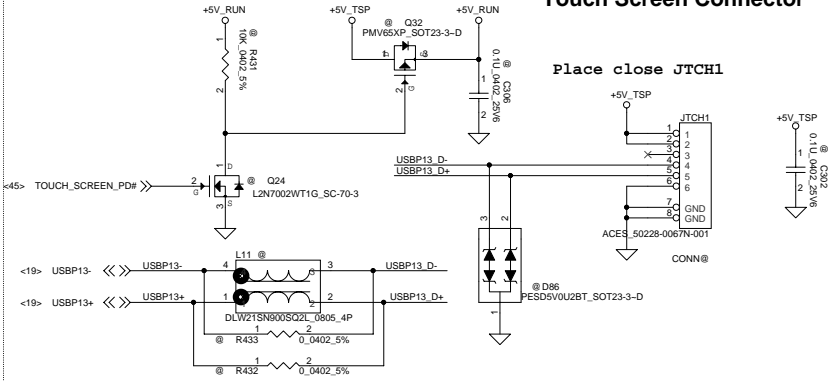
For Webcam



Webcam PWR CTRL



Touch Screen Connector



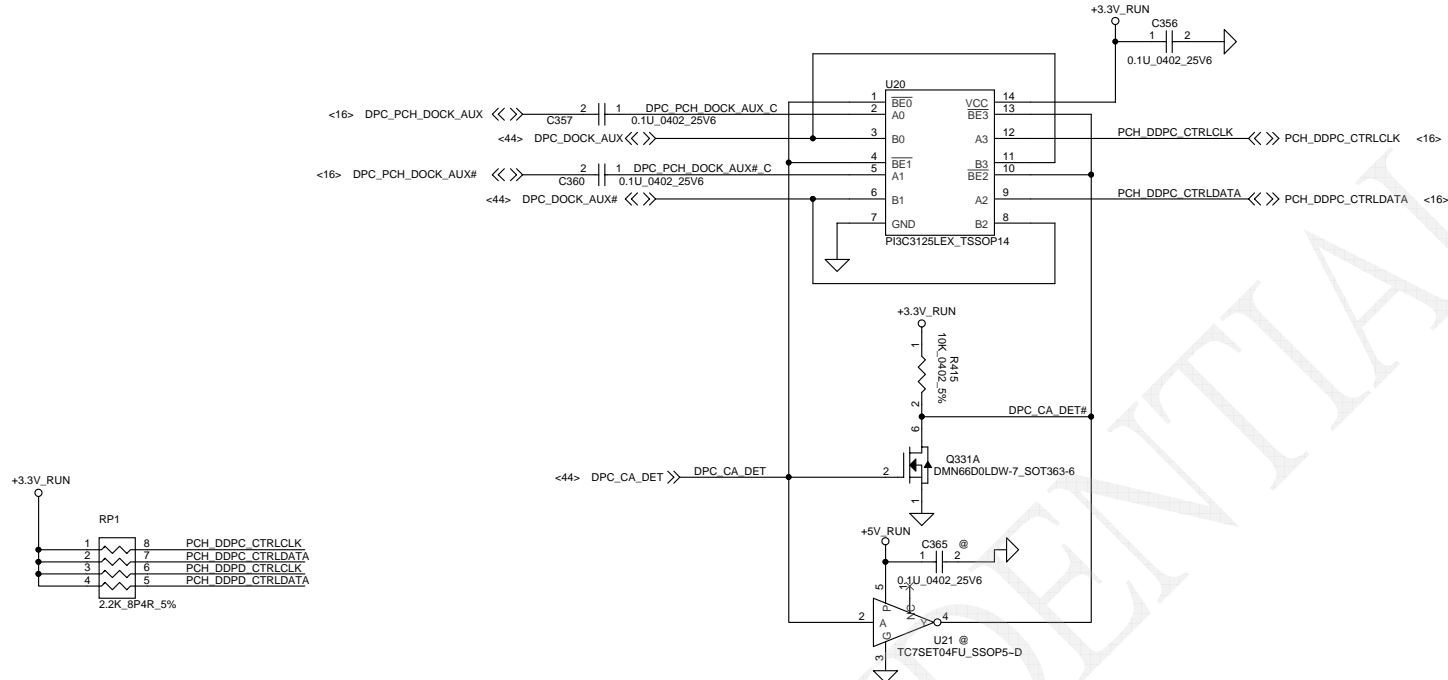
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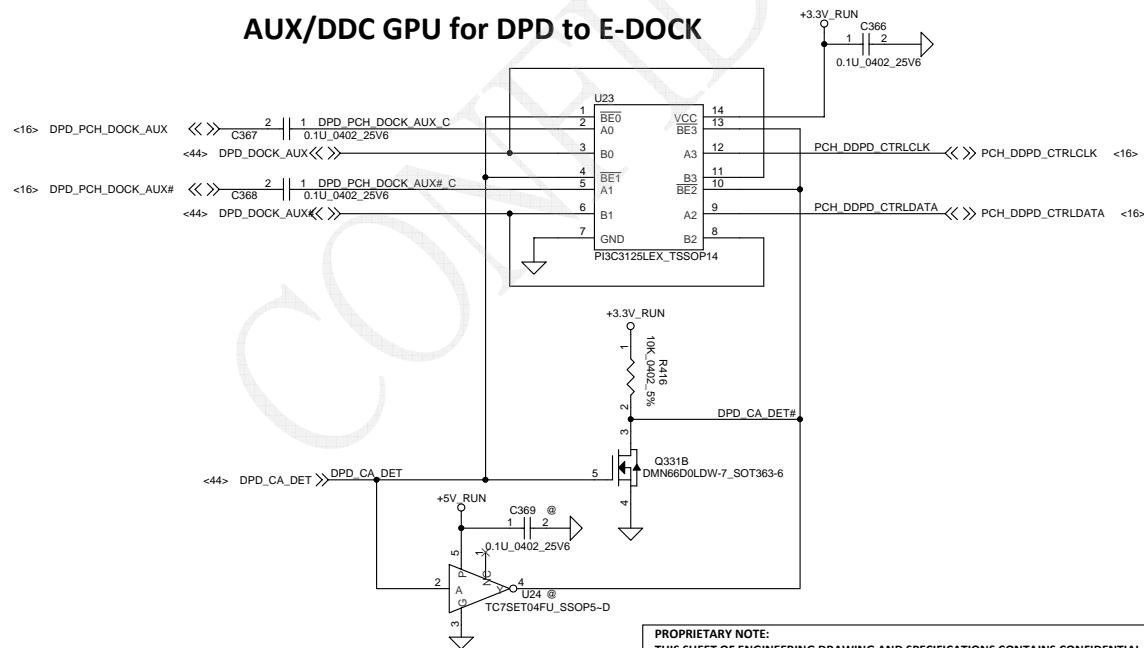
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AUX/DDC GPU for DPC to E-DOCK



AUX/DDC GPU for DPD to E-DOCK



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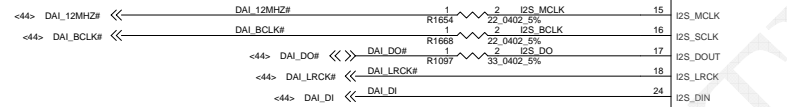
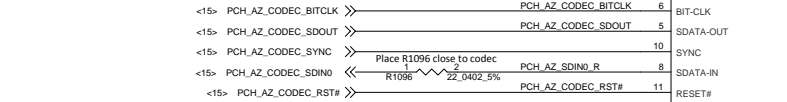
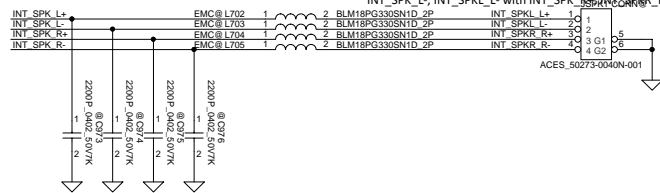
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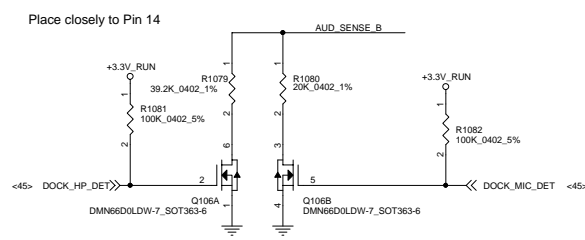
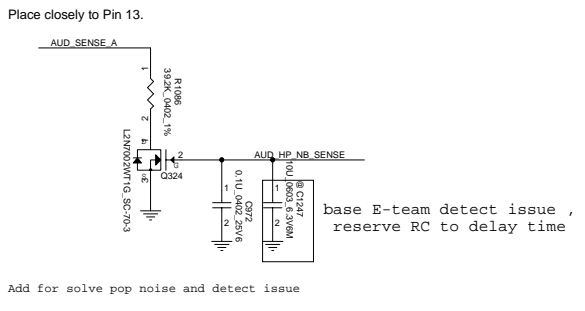
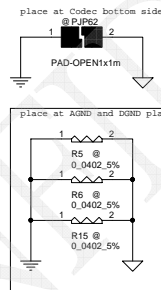
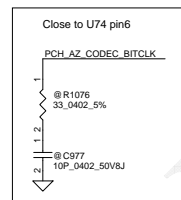
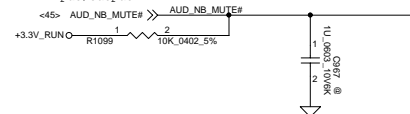
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Internal Speakers Header

INT_SPK_L+, INT_SPKL_L+ :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPKL_L- :40 mils trace, keep 10mils spacing
INT_SPK_R+, INT_SPKR_R+ :40 mils trace, keep 10mils spacing
INT_SPK_R-, INT_SPKR_R- :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPKL_L- with INT_SPK_R- and INT_SPKR_R+ keep 20mils spacing



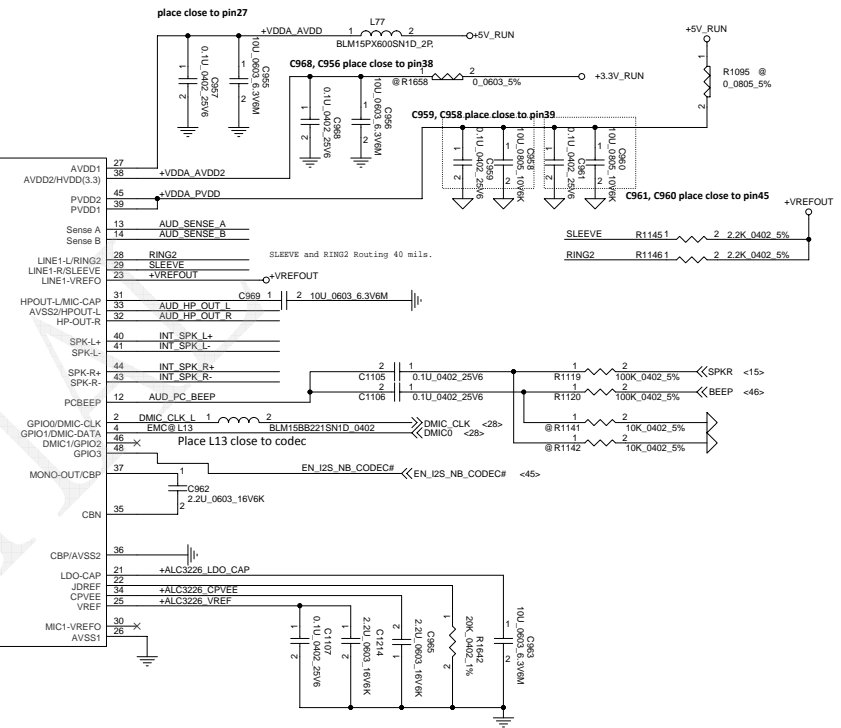
BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock
input/output



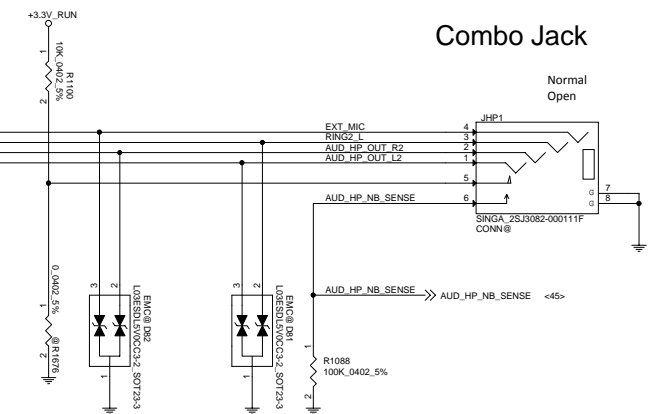
Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals.

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK



Combo Jack



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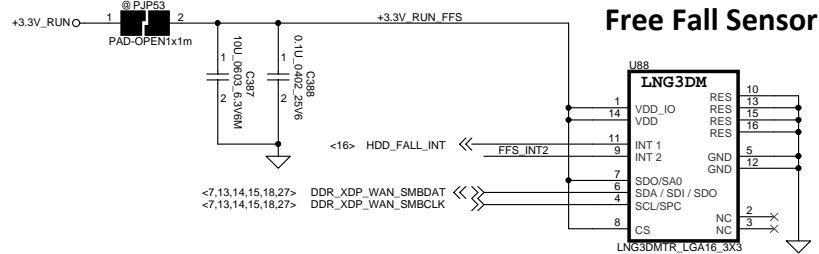
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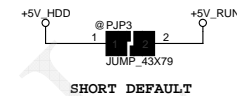
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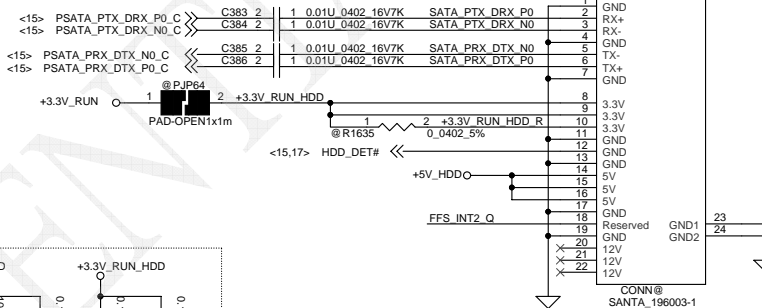
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HDD PWR



HDD CONN

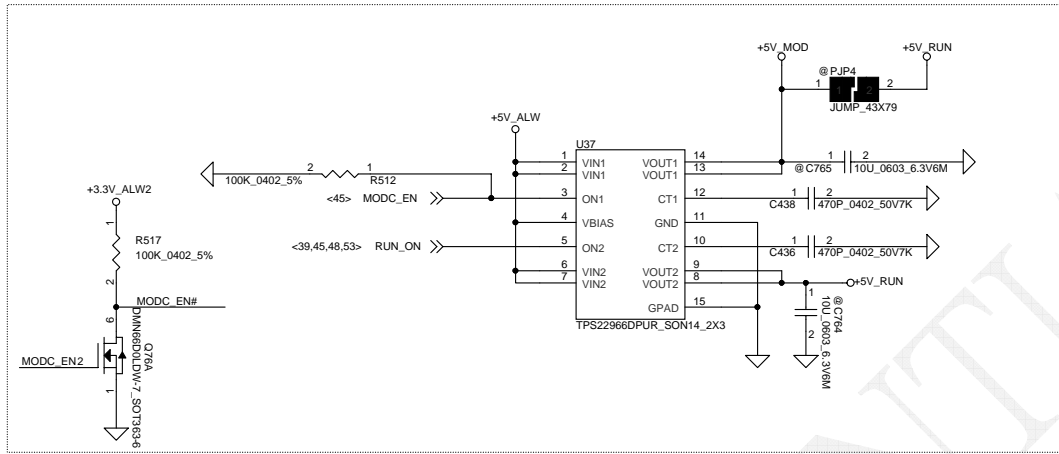


Main SATA +5V Default

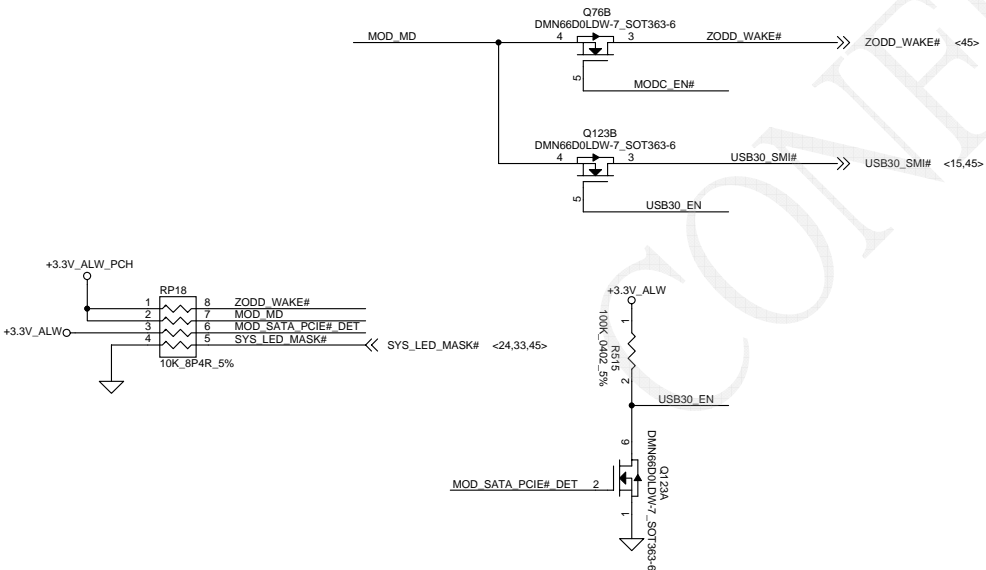
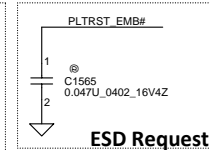
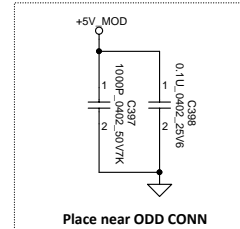
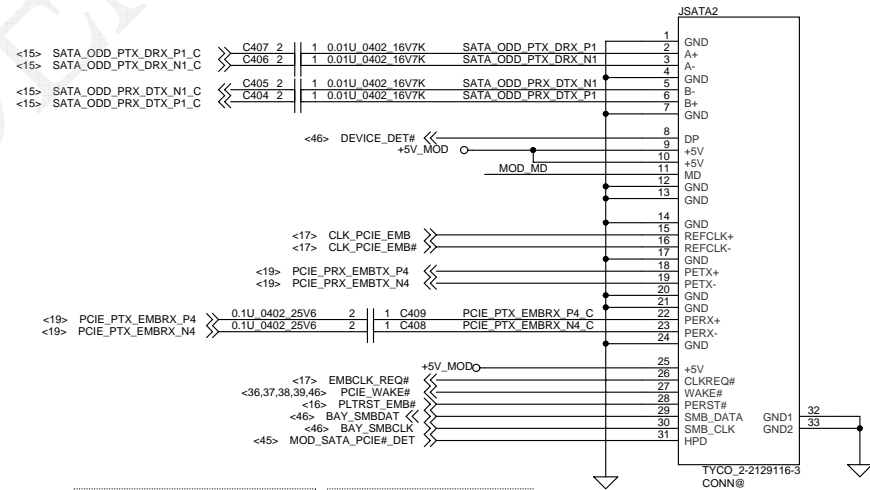
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+5V_MOD/+5V_RUN source



ODD CONN



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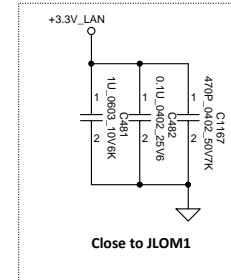
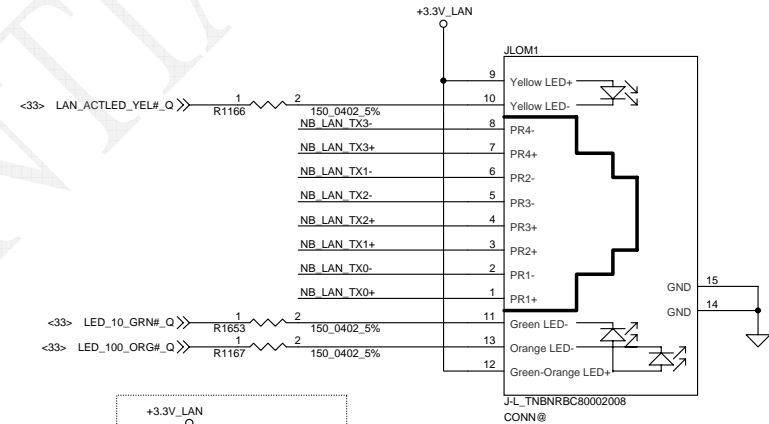
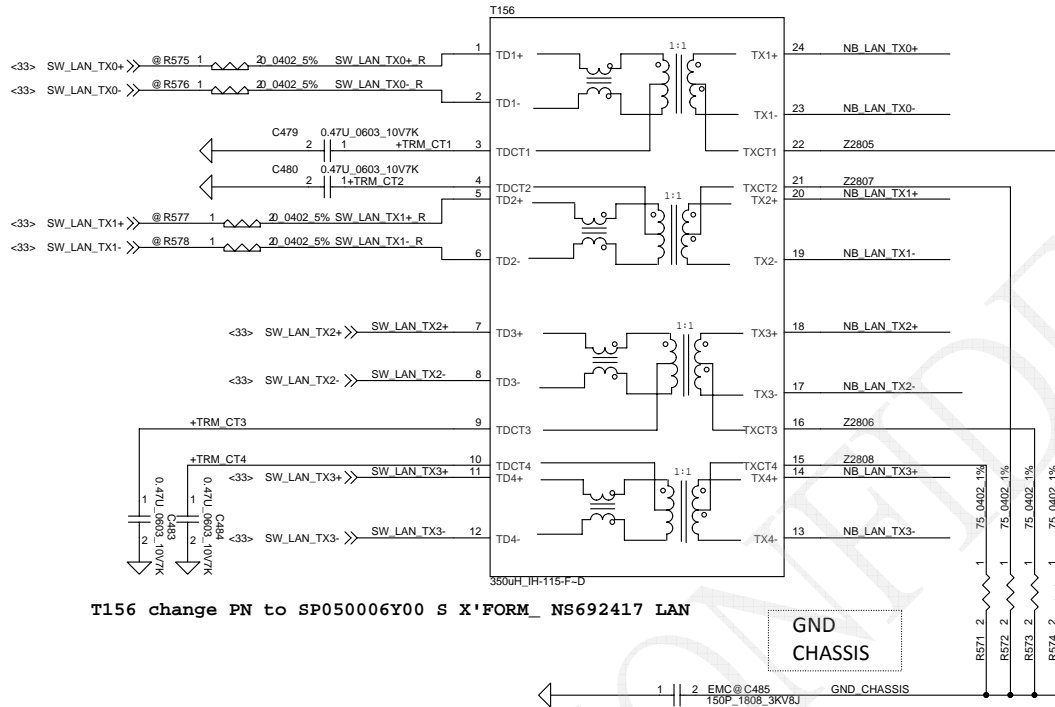
Compal Electronics, Inc.

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SW_LAN_TX0+ R	1	2	SW_LAN_TX0- R
@ C500	1	2	10P_0402_50V8J
SW_LAN_TX1+ R	1	2	SW_LAN_TX1- R
@ C501	1	2	10P_0402_50V8J

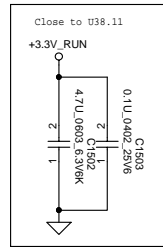
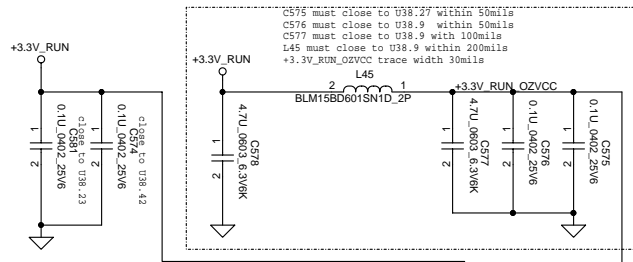


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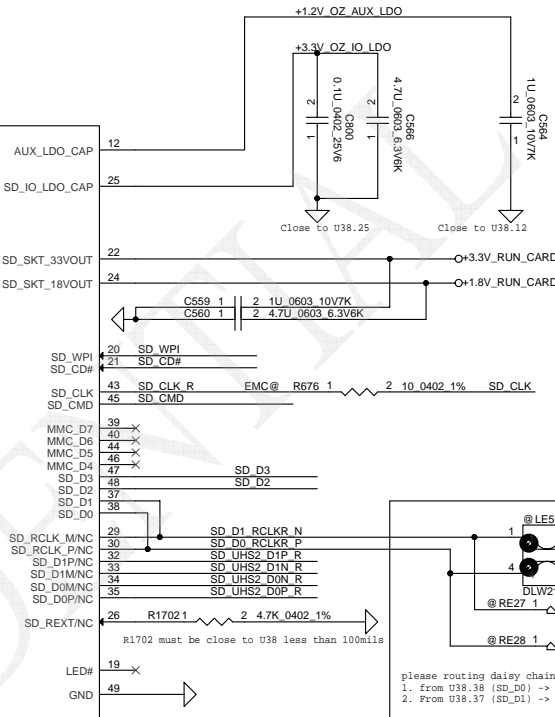
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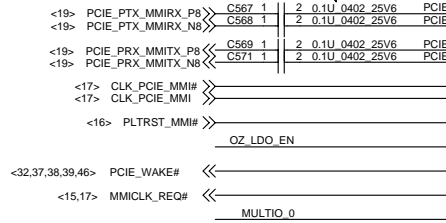
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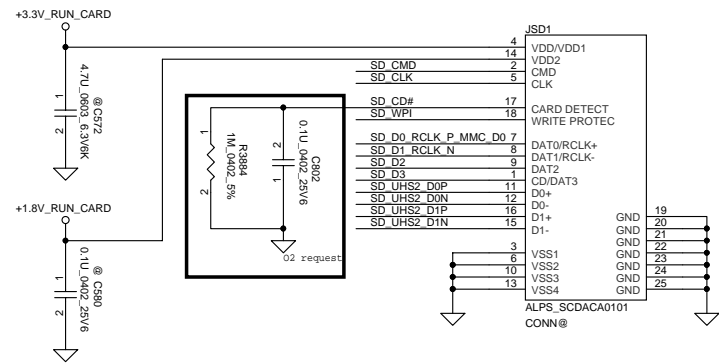
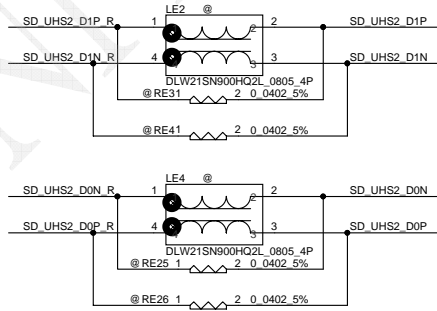
OZ777FJ2LN



please routing daisy chain
1. from U38.38 (SD_D0) -> U38.32 (SD_RCLK_P) -> LE5.4
2. From U38.37 (SD_D1) -> U38.33 (SD_RCLK_N) -> LE5.1



OZ777FJ2LN_QFN48_6X6



only for MMC/SD
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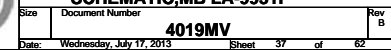
Compal Electronics, Inc.

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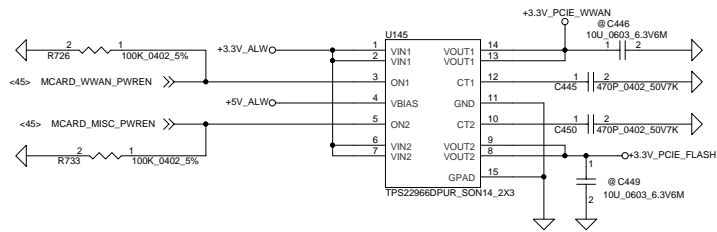
4019MV

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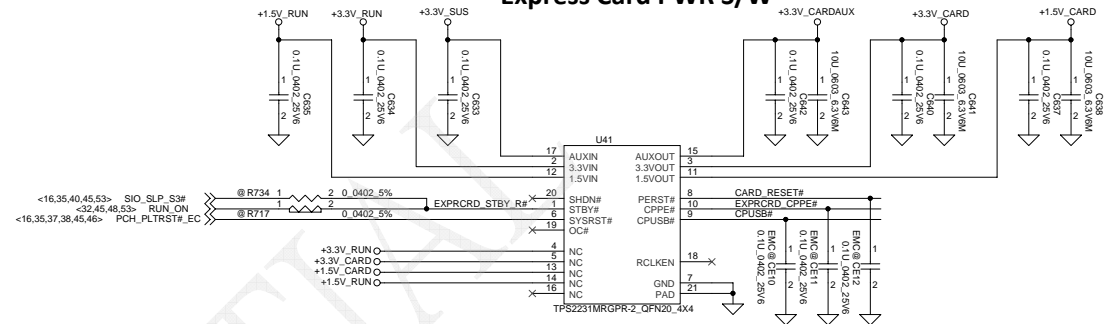
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[illegible]

+3.3V_PCIE_WWAN/+3.3V_PCIE_FLASH



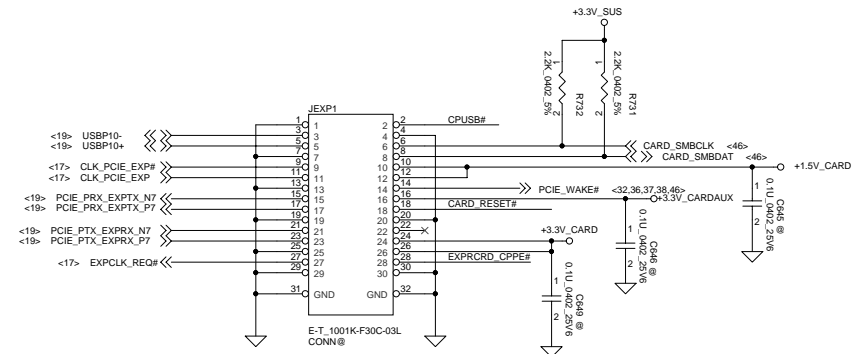
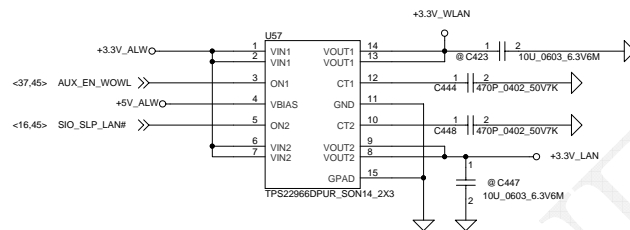
Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

Express Card Conn.

+3.3V_WLAN/+3.3V_LAN source



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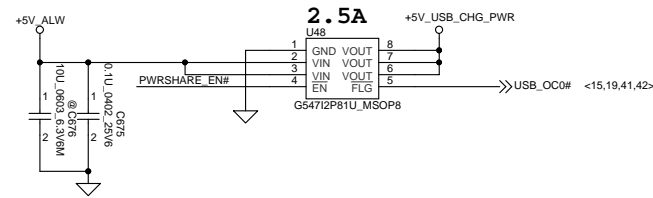
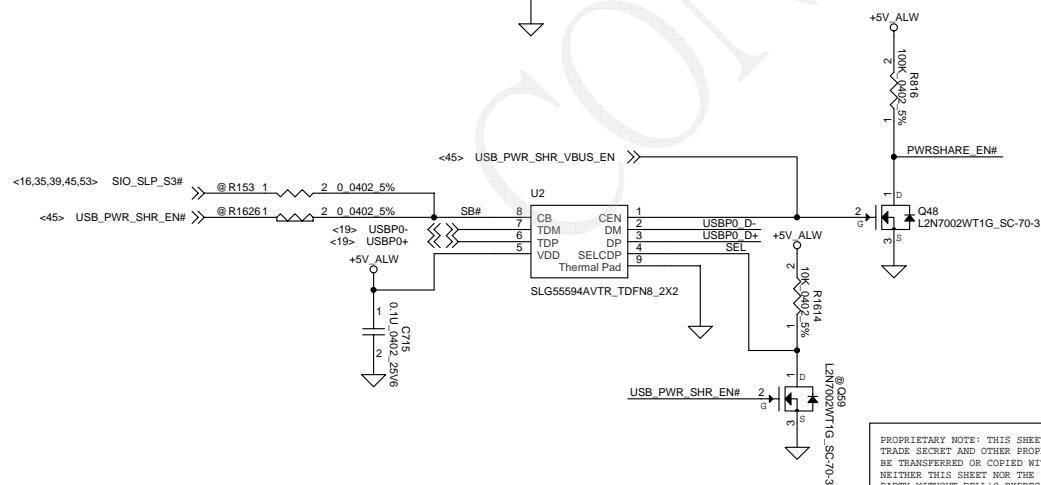
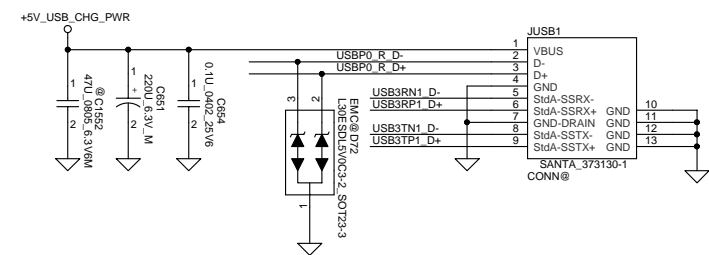
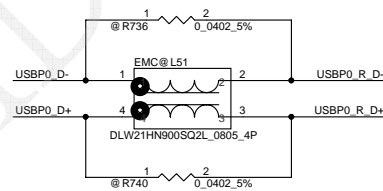
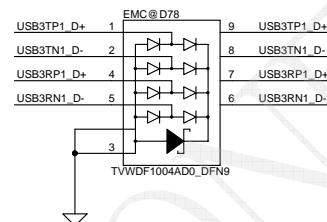
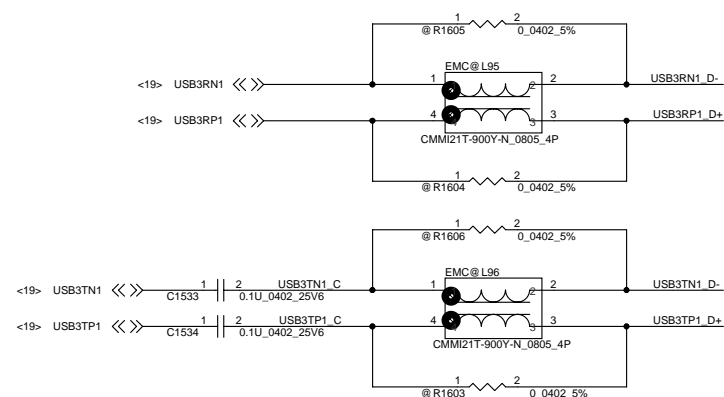
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Rear Side (JUSB1)



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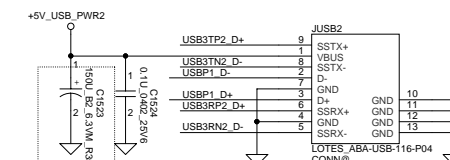
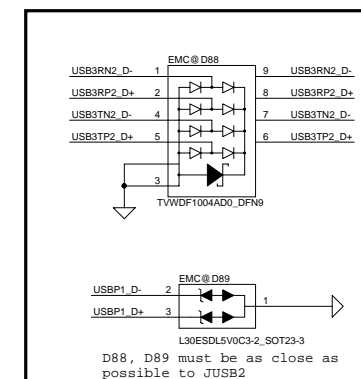
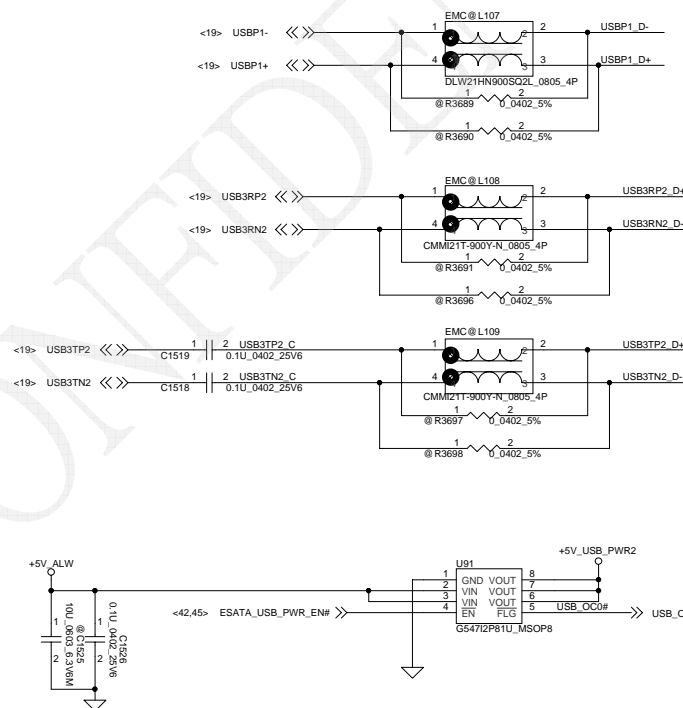
SCHEMATIC,MB LA-9931P

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Right Side Top (JUSB2)

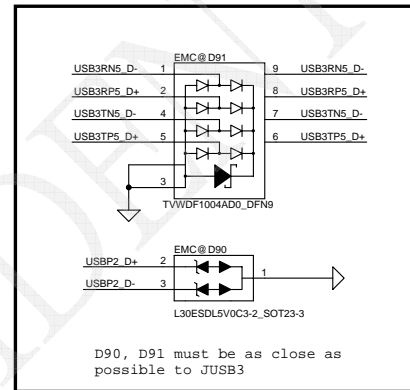
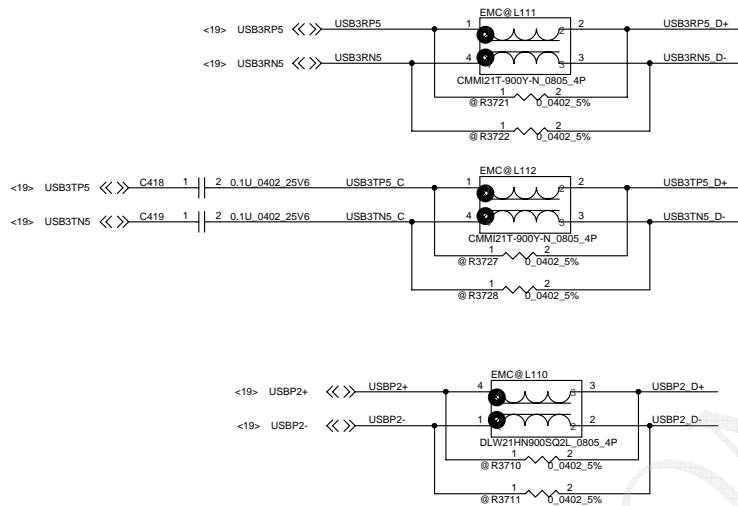


place C1523 between JUSB2 and JUSB3

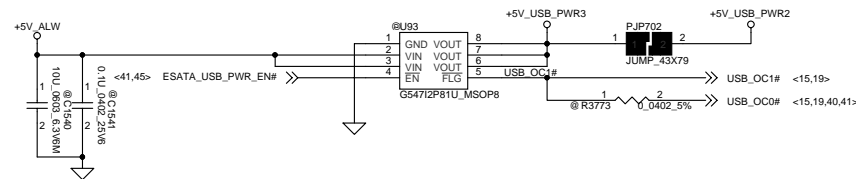
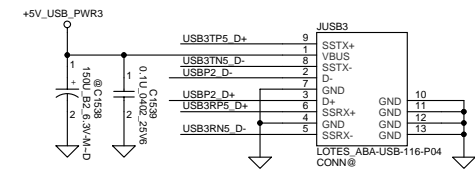
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Right Side bottom (JUSB3)



D90, D91 must be as close as possible to JUSB3

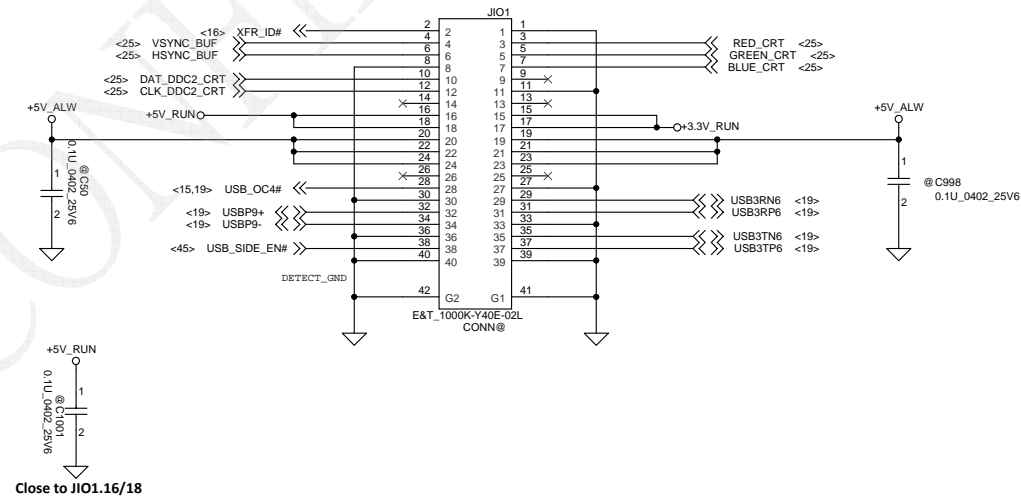


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I/O board CONN.



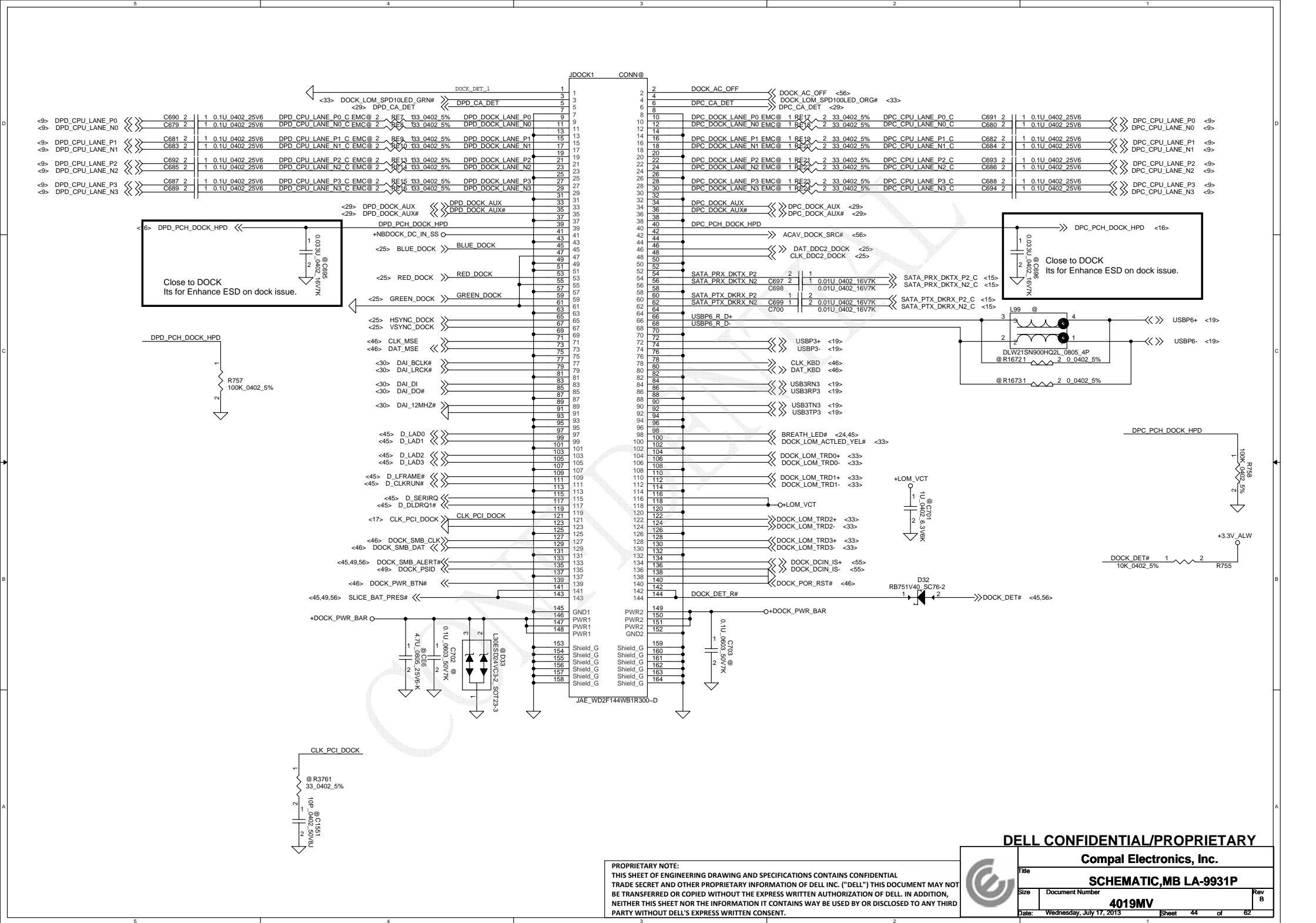
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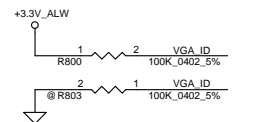
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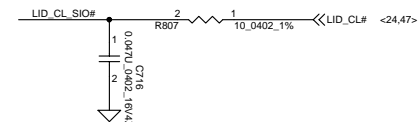
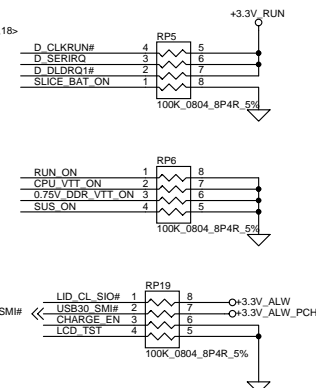
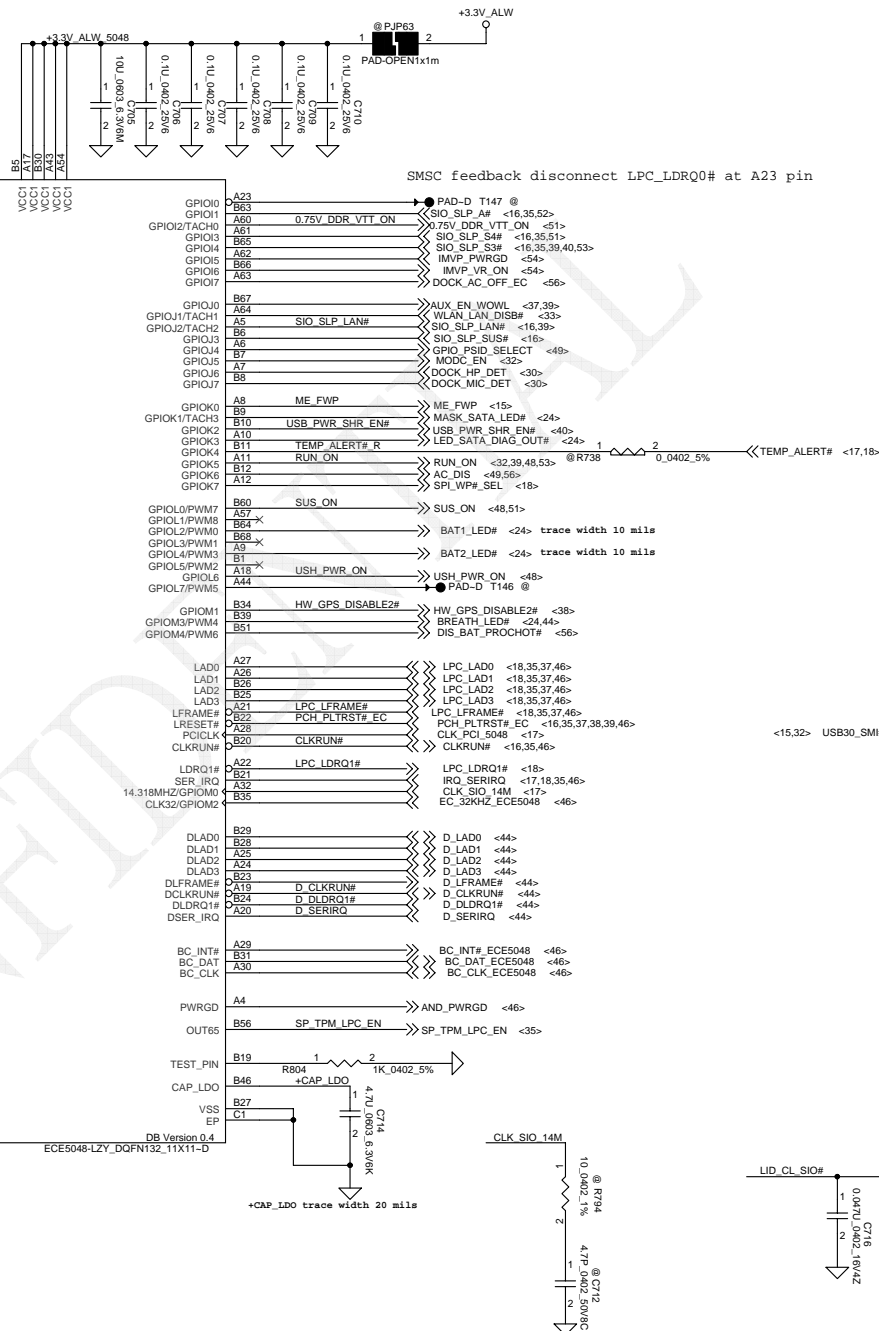
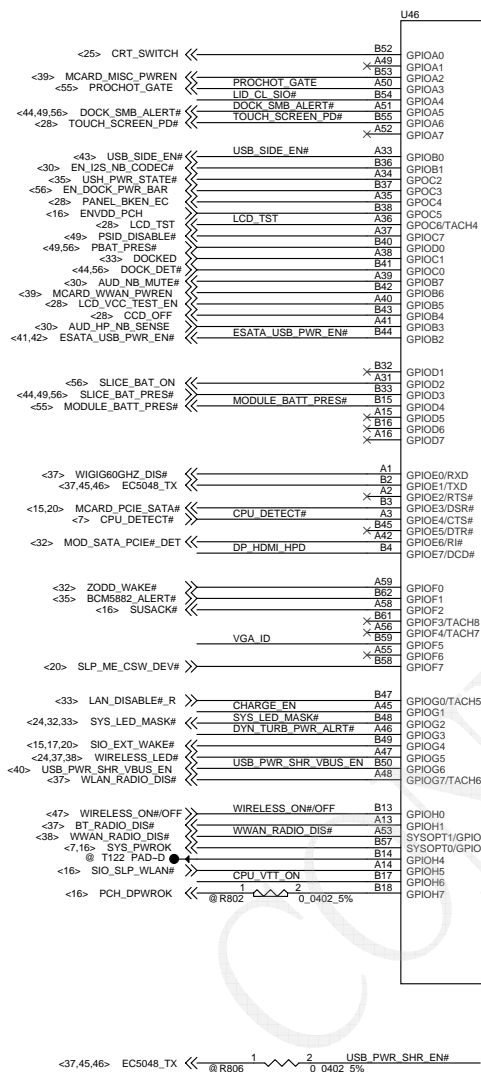
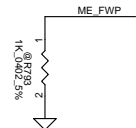
4019MV





	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.

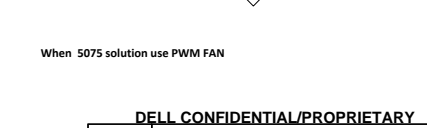
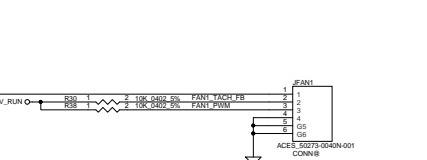
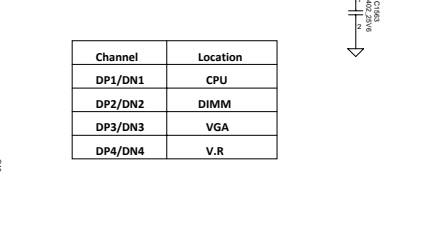
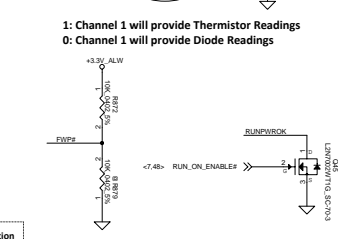
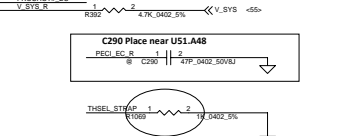
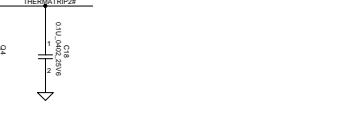
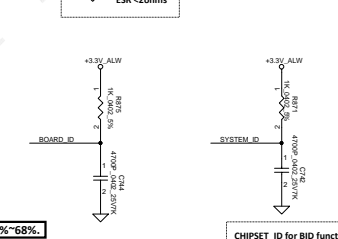
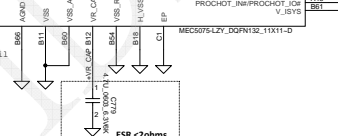
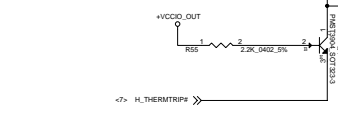
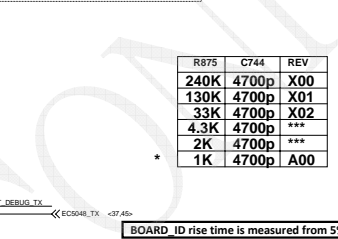
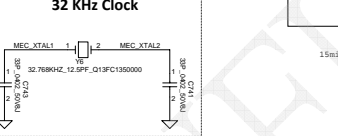
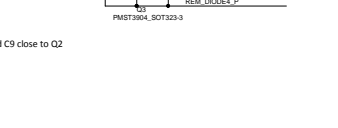
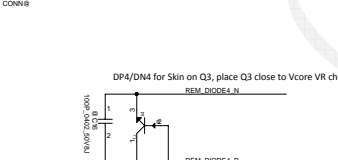
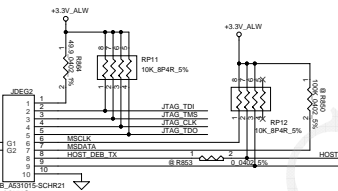
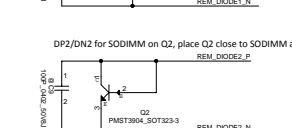
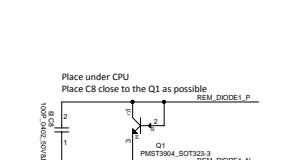
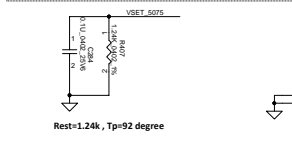
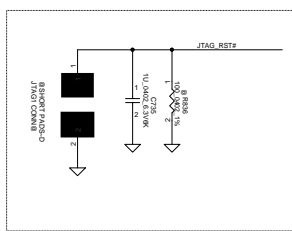
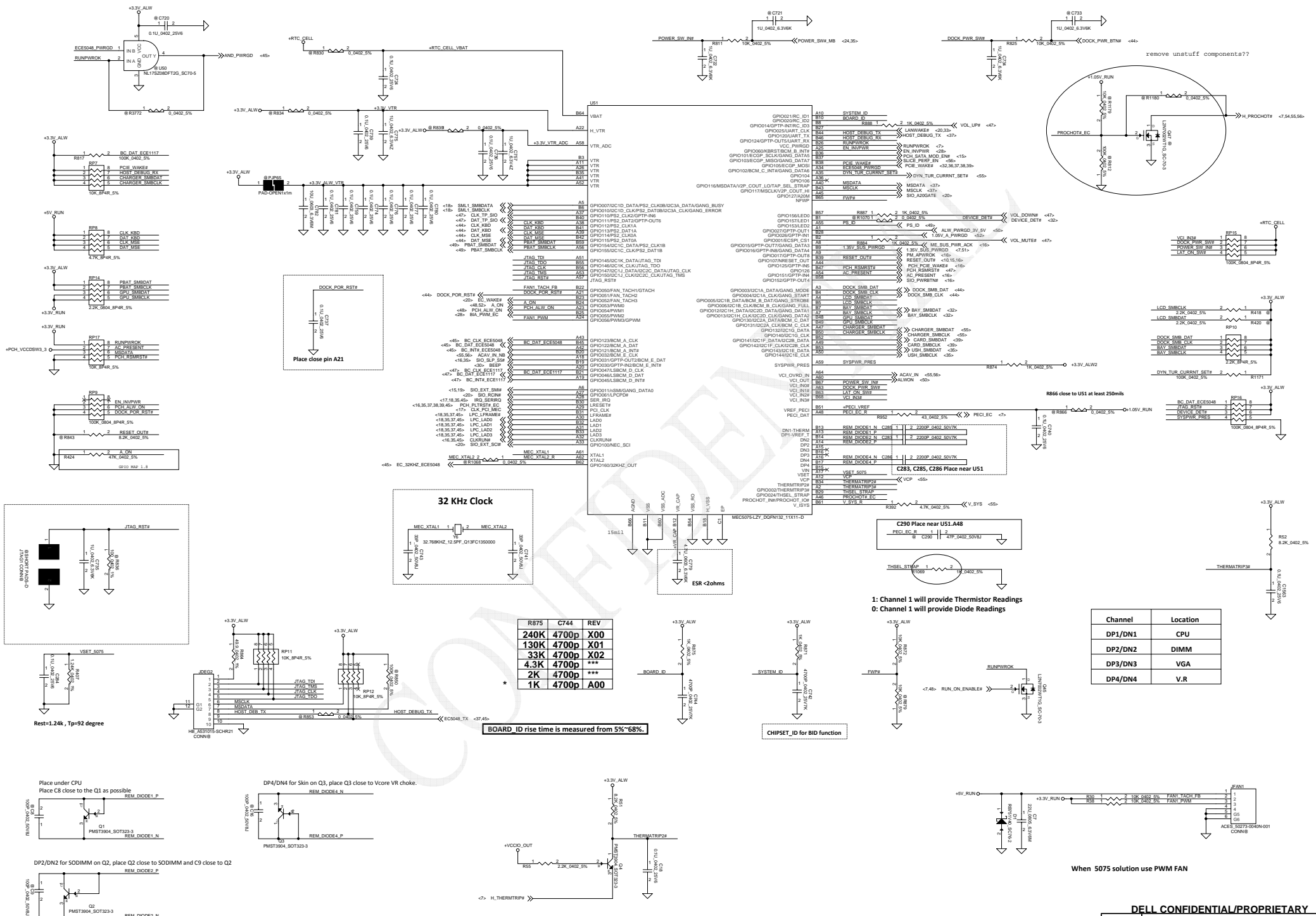


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Touch Pad

Media Board

Keyboard

Pinch: 1.0

The diagram illustrates the keyboard circuit connections. On the left, two power supply sections are shown: a 3.3V_ALW section with a 100µF 20V0 capacitor and a 5V_RUN section with a 100µF 20V0 capacitor. Both capacitors are connected to ground. The 3.3V_ALW line is connected to pin 4 of the JKB1 connector, and the 5V_RUN line is connected to pin 5. The data lines are connected to pins 2 and 3 of JKB1, which are labeled PS2_CLK_TS and PS2_DAT_TS respectively. The keyboard also provides two status signals: BC_INT#_ECE1117 and BC_DAT_ECE1117, which are connected to pins 6 and 7 of JKB1. The keyboard's ground is connected to pin 11 of JKB1, which is labeled GND. The keyboard's power and data lines are connected to the keyboard's pins 1 through 10. The keyboard's power and data lines are connected to the keyboard's pins 1 through 10. The keyboard's power and data lines are connected to the keyboard's pins 1 through 10.

Place close to JKB1

SNIFFER /Hall SENSOR BOARD

SNIFFER /Hall SENSOR BOARD

3.3V ALW

10k

3.3V ALW

LID_CL#

WIRELESS_ON#/OFF#

GND

JSF1

HB_A090620-SAHR21
CONN@

WIRELESS_ON/OFF#:
LOW: ON (Default)
HIGH: OFF

(PITCH 0.5) Right side LED

1 2 3 4 5 6 7 8

JLED1

1 2 3 4 5 6 7 8

BATT_YELLOW# BATT_WHITE# SATA_LED WLAN_LED

<24> <24> <24> <24>

WLAN_LED

HB_A520620-SCHR22


CONN@

+5V_ALW

C100A

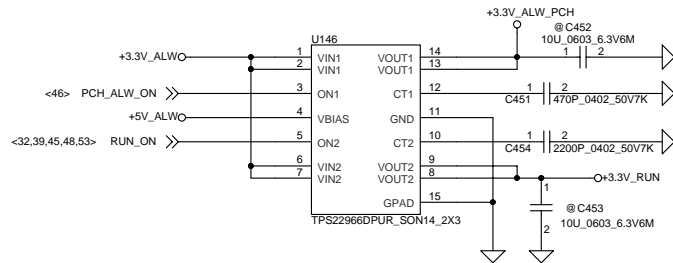
0.1uF 0402 25V6

Close to JLED2

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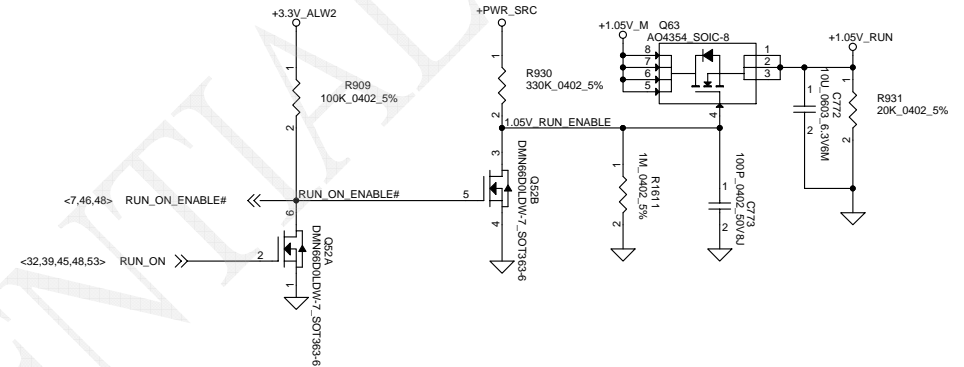
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+3.3V_ALW_PCH/+3.3V_RUN Source

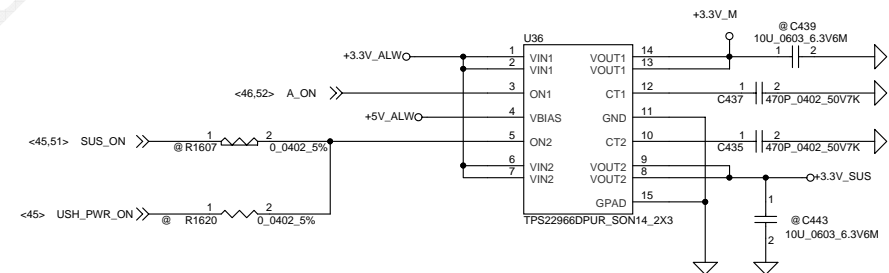


SI4164DY		
VDS	RDS(on)	ID(A)
30	0.0032ohm at VGS=10V	30A
30	0.0039ohm at VGS=4.5V	26.3A

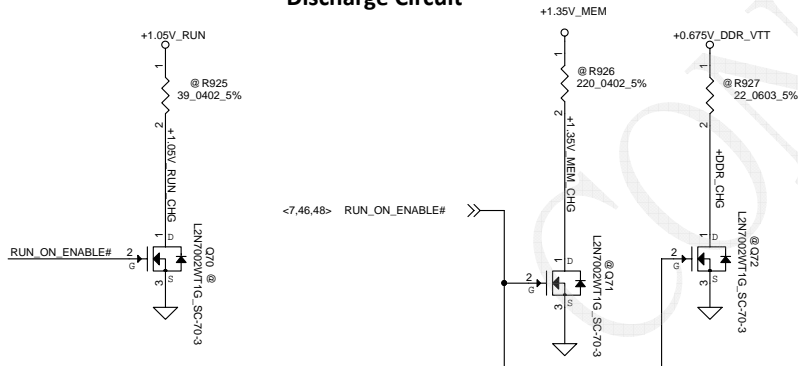
+1.05V_RUN Source



+3.3V_M/+3.3V_SUS source



Discharge Circuit



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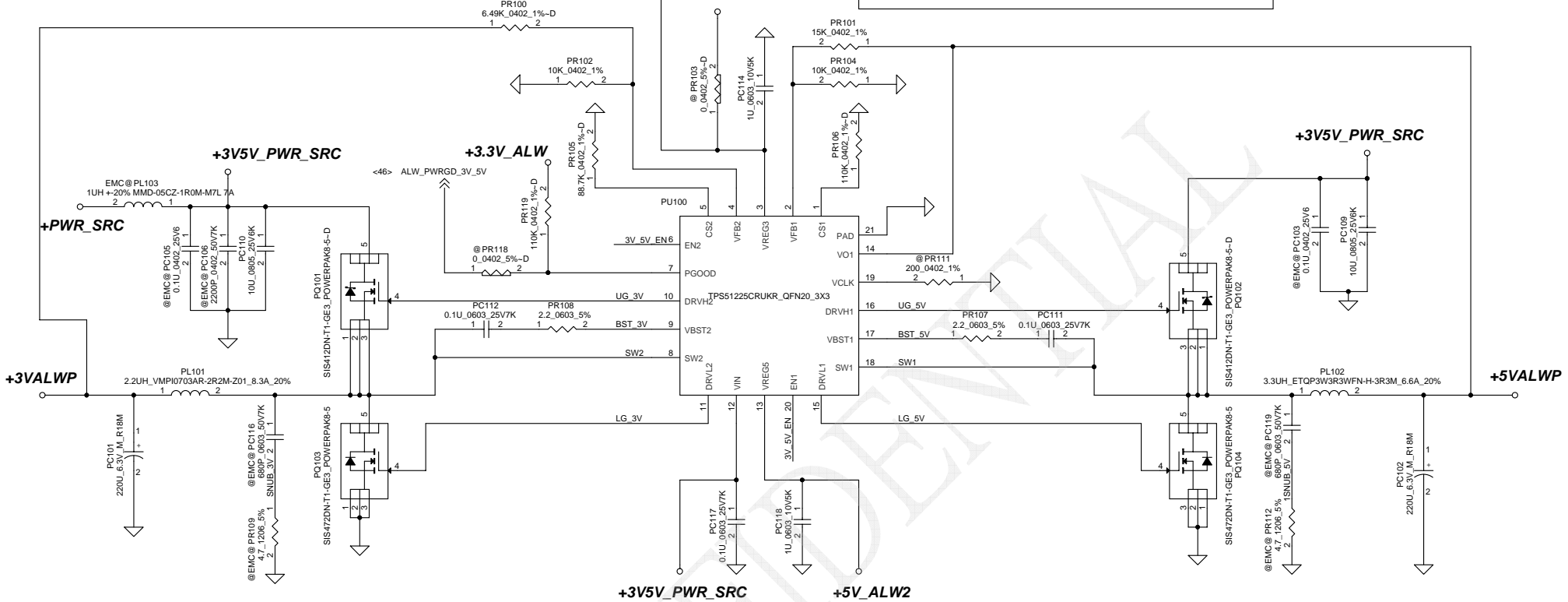
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$$VFB2=2V, PR100=(V_{out}-0.5*V_{ripple}-2)/2*PR102$$

+3.3V_ALW2

+3.3V_RTC_LDO

$$VFB1=2V, PR101=(V_{out}-0.5*V_{ripple}-2)/2*PR104$$




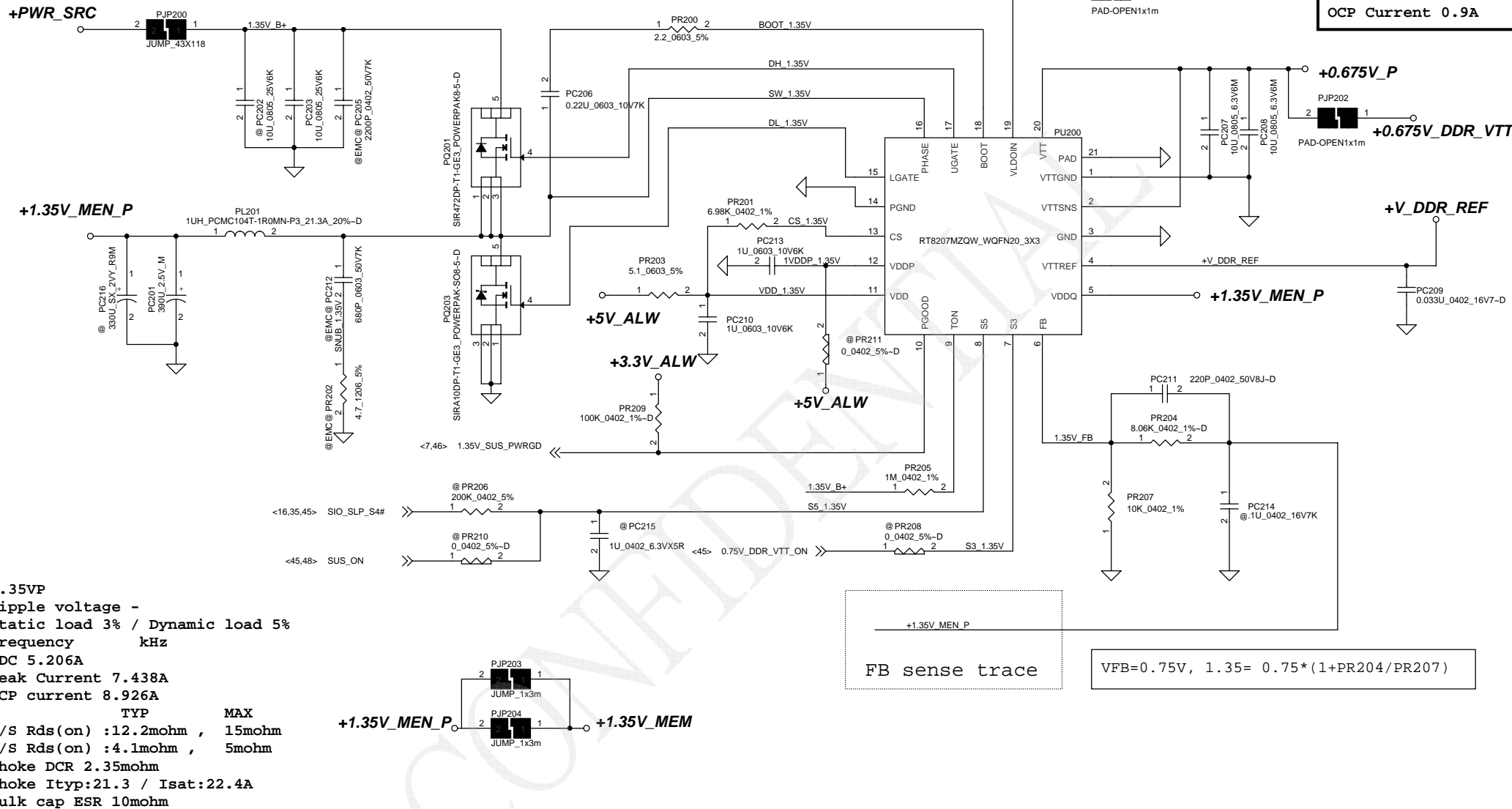
3VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 350kHz
TDC 5.099A
Peak Current 7.285A
OCP current 8.742A
TYP MAX
H/S Rds(on) 24mohm , 30mohm
L/S Rds(on) 10.3mohm , 12.4mohm
Choke DCR Max:17mohm
Choke Ityp:8.3A / Isat:10.8A
Bulk cap ESR 18mohm

5VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 300kHz
TDC 6.075A
Peak Current 8.679A
OCP current 10.415A
TYP MAX
H/S Rds(on) 24mohm , 30mohm
L/S Rds(on) 10.3mohm , 12.4mohm
Choke DCR Max:28mohm
Choke Ityp:6.6A / Isat:8.2A
Bulk cap ESR 18mohm

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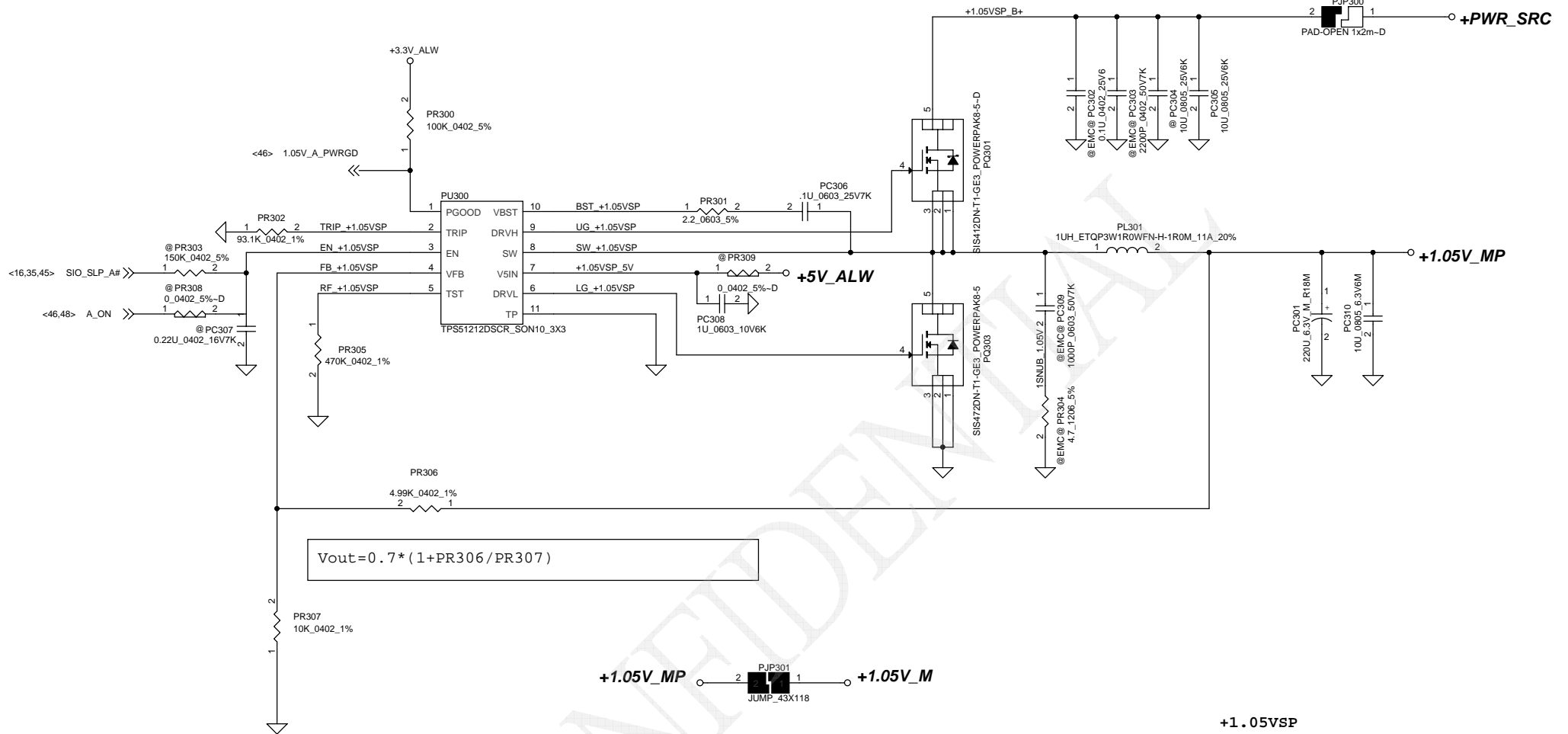


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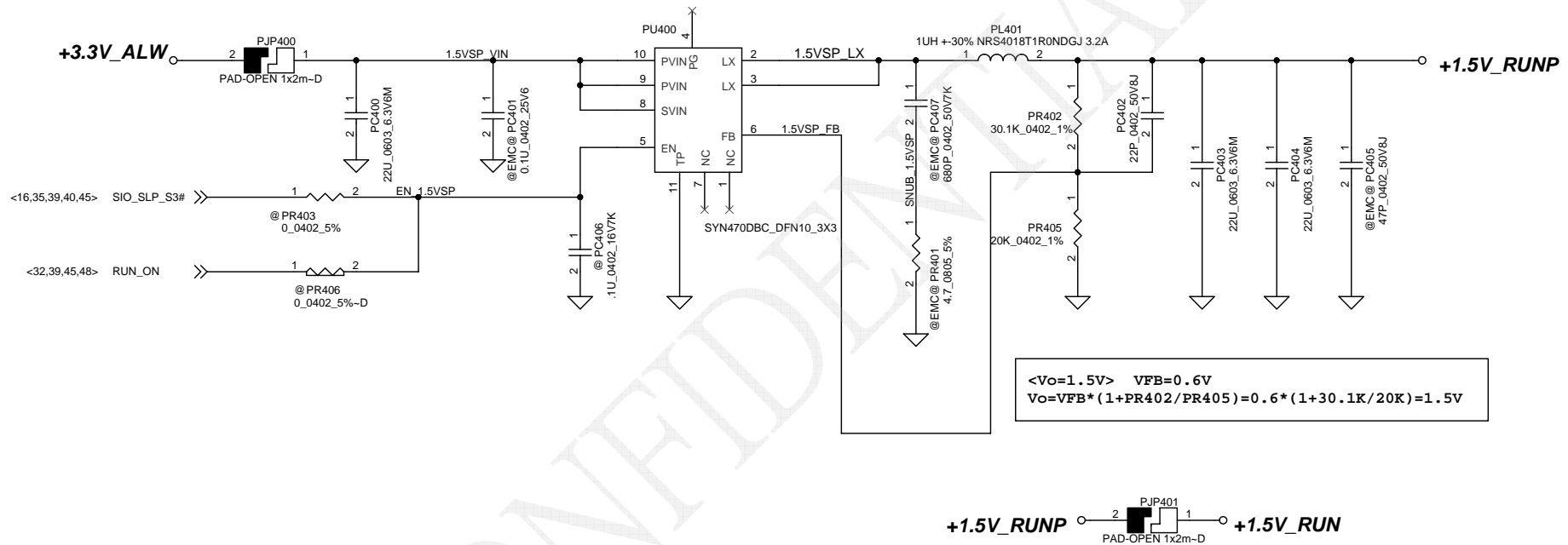
+1.05VSP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 290kHz
 TDC 4.659A
 Peak Current 6.523A
 OCP current 7.828A
 TYP MAX
 H/S Rds(on) 24mohm , 30mohm
 L/S Rds(on) 10.3mohm , 12.4mohm
 Choke DCR 11mohm
 Choke Ityp:11A / Isat:14.5A
 Bulk cap ESR 18mohm

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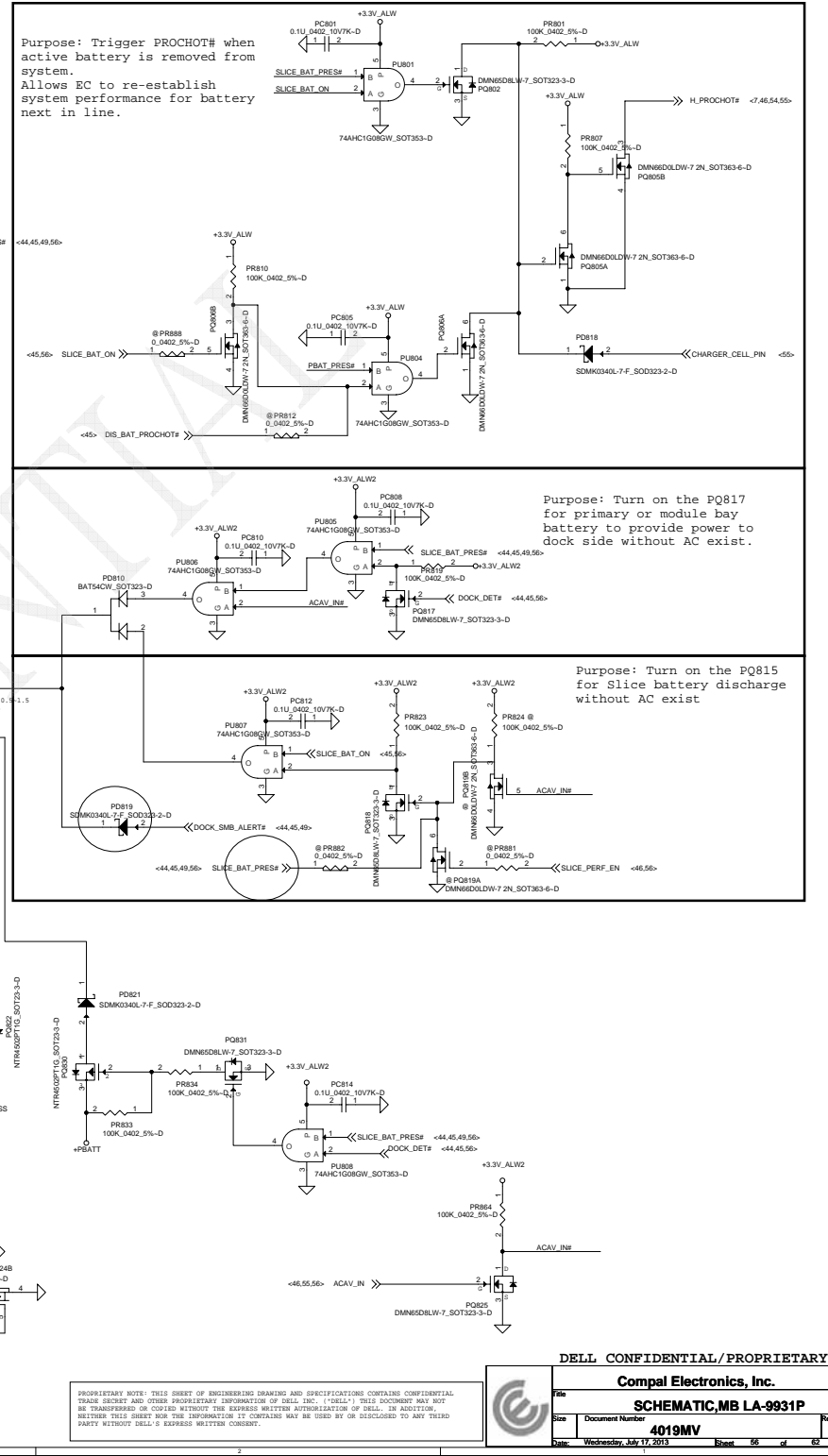
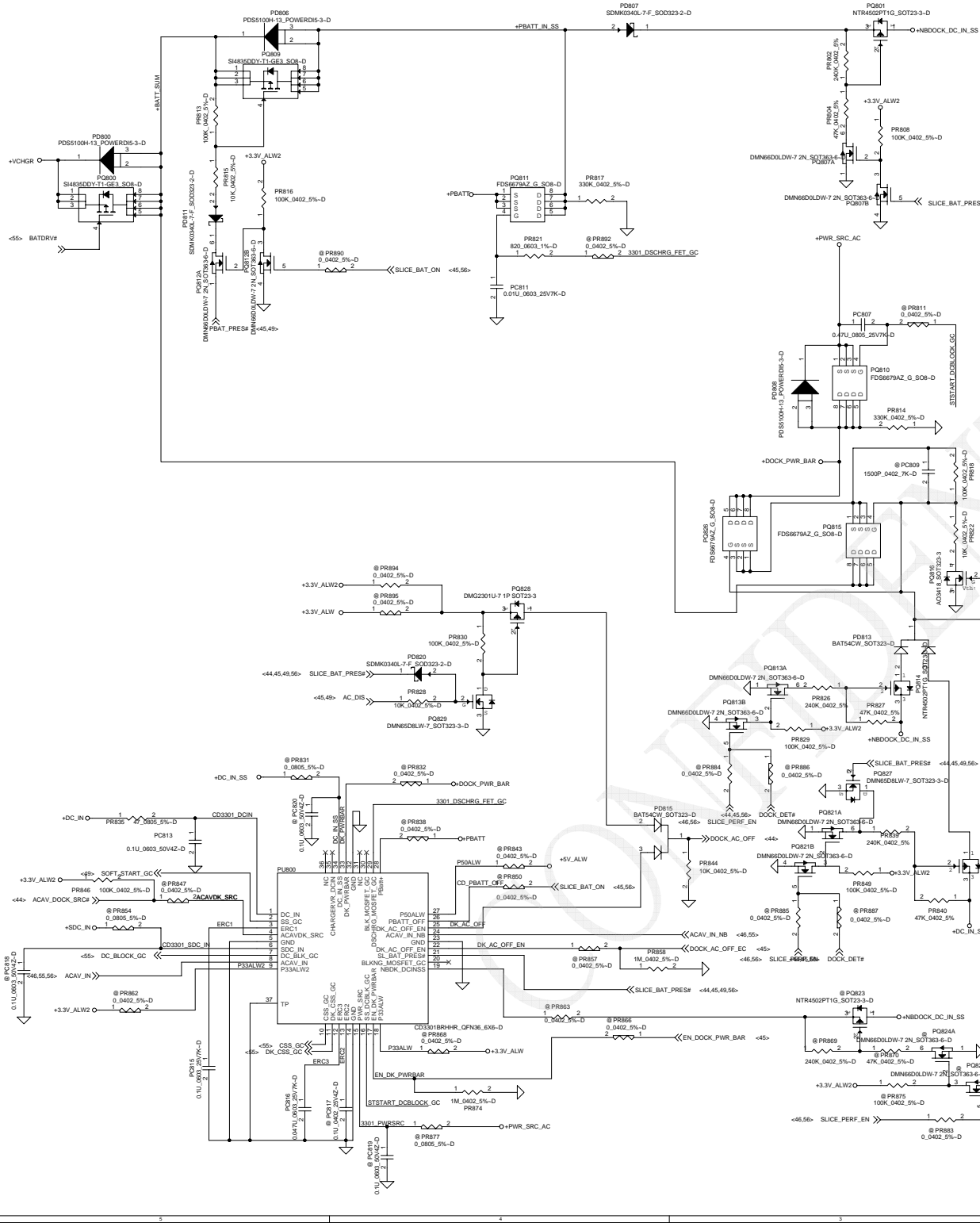
+1.5VSP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 1MHz
 TDC 1.329A
 Peak Current 1.899A
 OCP current 2.279A
 Choke DCR 27mohm
 Choke Ityp:3.2A / Isat:4A



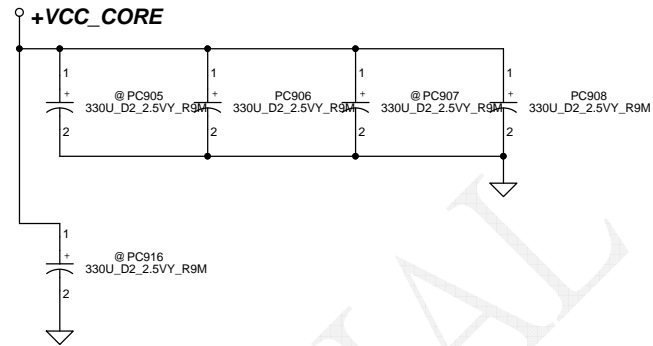
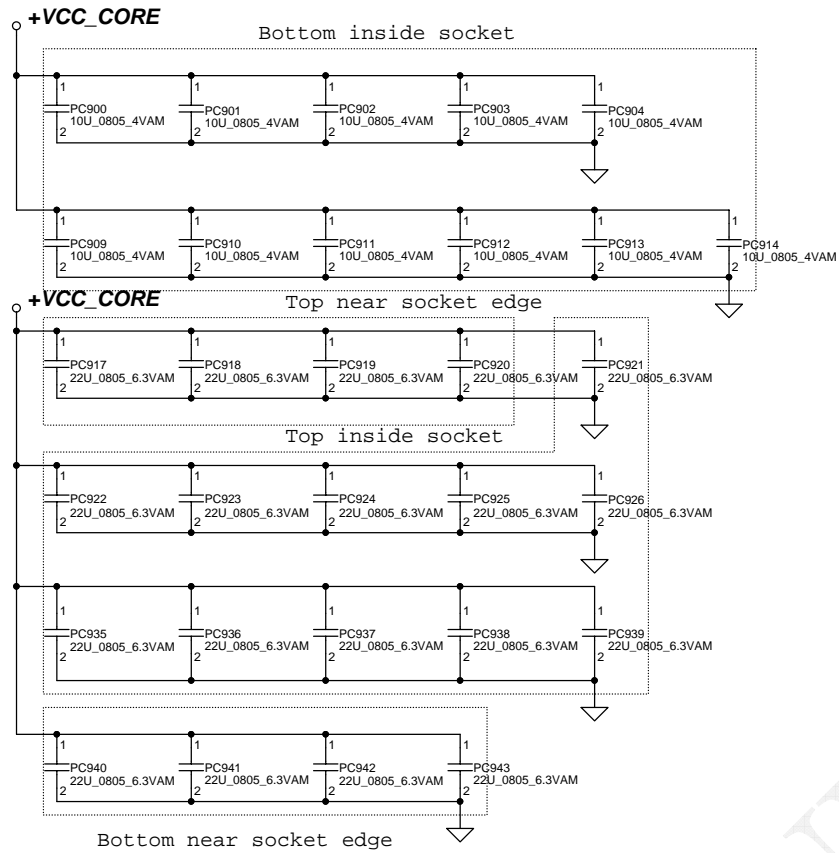
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Based on PDDG rev 1.1 Table 5-1.




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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	55	Charger	1/8	TI	Change cell pin pull high reference voltage from +3.3V_ALW to BQ24715_REGN	Depop PR720 and pop PR746	X01
2	55	Charger	1/8	Compal	Reduce adapter current ripple	PC724,PC728,PC712,PC713,PC714,PC734 pop 22uF cap	X01
3	54	VCC_CORE	1/8	Compal	Reduce adapter current ripple	Add input jump PJP500 and unpop PL504, PC516 pop 470pF	X01
4	55	Charger	1/8	Compal	Fine tune H_PROCHOT# response time.	Add 0402 cap PC736(1.2nF) on PU701 pin1	X01
5	55	Charger	1/8	Compal	Control H_PROCHOT# when AC removed.	Add PR727(0 ohm) and MODULE_BATT_PRES# connect to PU701 pin1	X01
6	54	VCC_CORE	1/8	Compal HW	Reduce noise on +VCCIO_OUT.	Add 1uF cap (PC548) on +VCCIO_OUT	X01
7	55	Charger	1/8	Compal	For Input current sense stabilize.	PC703 change from 0402 0.1uF to 0603 1uF	X01
8	56	Selector	1/8	Compal	For undock shutdown issue.	Add PQ827 and gate connect to SLICE_BAT_PRES#.	X01
9	55	Charger	1/8	Compal	To prevent charger into sleep mode when dual AC transient.	PC707 change from 1uF to 10uF.	X01
10	55	Charger	1/8	Compal	Improve ACAV_IN_NB ref voltage accuracy.	PR733 connect to +3.3V_ALW2. PR740 change from 12K to 10K PR733 change from 130k to 48.8k	X01
11	54	VCC_CORE	1/8	Intersil	Fine tune IMON, OCP, Iout offset.	Add PR558 4.99M on ISUMP to GND. PR535 change from 432 to 499. PR521 change from 95.3k to 97.6k. PC500 change from 0.01u to 1000p	X01
12	55	Charger	1/9	Compal	Fine tune ACOK response time.	PC708 change from 0.01uF to 0.1uF	X01
13	49 56	DCIN selector	1/9	Compal	GPIO net - AC_DIS# is high active. Corrent net name.	AC_DIS# cahnge to AC_DIS.	X01
14	55	Charger	1/9	Compal	Improve current sense accuracy.	PR744=44.2ohm PR736=59ohm	X01
16	56	Selector	1/9	Compal	AC_DIS circuit modify to improve output voltage level.	Add PD820,PQ828,PQ829,PR895.	X01
17	52	1.05V_VM	1/11	Compal	Improve output ripple voltage.	Add 10uF(PC310) on output.	X01
18	56	DCIN	1/14	Compal	To prevent PD2 damage issue, ESD team suggest pin5 connect to VCC.	PD2 pin5 connect to +3.3V_ALW, Add PR27 0 ohm PD2 change from NXP(SC300001100) to AMC(SC300001G00)	X01
19	55	Charger	1/17	Compal	Adapter protect from rating+0.75A to 2A.	PR730 change from 150k to 249k PR731 change from 66.5K to 162K unpop PR727	X01
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Version Change List (P. I. R. List)

	Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
D	1	49	DCIN	4/2	Compal ESD	PD2 ESD diode damage issue.	ESD diode change from dual package to single package(PD2,PD4)	X02
	2	All	All	4/8	Compal	0 ohm resistor change to short pad.	PR26,PR103,PR110,PR118,PR208,PR210,PR211,PR308,PR309,PR406,PR511,PR520,PR524,PR526,PR548,PR700,PR702,PR704,PR705,PR709,PR710,PR717,PR718,PR719,PR724,PR737,PR745,PR811,PR812,PR832,PR838,PR843,PR847,PR850,PR857,PR862,PR866,PR868,PR882,PR886,PR887,PR888,PR890,PR892,PR895	X02
	3	49	DCIN	4/11	Compal	Saving space.	PL4 change from 0603 to 0402.	X02
C								
B								
A								

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37,45,46	HW	12/10/2012	Compal	Change R-Pak package.	Change RP3,RP4,RP5,RP6,RP9,RP13 P/N to SD309100380 (Change Package from 1206 to 0804)	X01
2	46	HW	12/10/2012	Compal	Change R-Pak package.	Change RP8 P/N to SD309470180 (Change Package from 1206 to 0804)	X01
3	35	HW	12/10/2012	Compal	Change New TPM Chip	Change U39 P/N to SA00004WQ40 (AT97SC3204-DX4A12-ABF)	X01
4	28	HW	12/18/2012	Compal	Impact SMT DFX stilt and solder risk.	Change JLVDS1 P/N from SP01001BS00 to SP01001BT00	X01
5	20,35	HW	12/21/2012	DELL	Update GPIO map to rev 3.0C	Reserve PCH GPIO 22 for moving SP_TPM_LPC_EN from OUT65 and add PD 100k(RH332)	X01
6	30	HW	12/21/2012	Compal	Remove non-pop item	Remove R3730	X01
7	46	HW	12/21/2012	DELL	Update GPIO map to rev 3.0C	Add a 0ohm resistor R3772 to short RUNPWROK and AND_PWRGD	X01
8	28	HW	12/21/2012	DELL	ATG droop	Remove ATG config 1@,2@	X01
9	40	HW	12/26/2012	Compal	Support Samsung Galaxy Tab charger in S3.	Change USB charger P/N from SLGC55584AVTR to SLG55594AVTR	X01
10	38	ME	01/02/2013	Compal	JSIM1 BOSS hole update from 3.55mm to 1.7mm	Change JSIM1 P/N from 159-1000302600 to 159-1000302602	X01
11	47	ME	01/03/2013	Compal	JSF1 pitch change from 0.5mm to 1.0mm	Change JSF1 P/N from A520620-SCHR22 to A090620-SAHR21	X01
12	30	HW	01/03/2012	COMPAL	Follow Realtek recommend circuit	1.Change R1119 ,R1120 to 100K 2.Change R1677 R1679 to 9.1 ohm 3.Change C958,C960 from 0603 to 0805	X01
13	28	HW	01/04/2013	COMPAL	Import U148 of 2nd source	U148 pin4 connect to +3.3V_ALW and remove C33	X01
14	15,17,18, 20,46	HW	01/04/2013	COMPAL	Import R-Pak	R820,R818,R829,R822 change to RP14 R1125,R810,R1156,R819 change to RP15 R814,R920,R870,R876 change to RP16 RH168,RH329,RH125 change to RPH18 R799,R835,R892,R869 change to RP17 RH138,RH136,RH257,RH201 change to RPH19 RH133,RH141,RH143,RH36 change to RPH20 RH122,RH166,RH171,RH217 change to RPH21 R1183,R513,R510,R775 change to RP18 R514,R767,R3,R805 change to RP19 R728,R739,R737,R716 change to RP20	X01
15	46	HW	01/07/2013	COMPAL	Change Board ID from X00 to X01	Change R875 from 240K to 130K	X01

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